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TECHNICAL REFERENCE

TYPE 4038

MULTIPROCESSOR COMMUNICATIONS ADAPTER

The Multiprocessor Communications Adapter (MCA) facilitates the interconnection of up to fifteen Nova-line computers into a multiprocessor system by permitting blocks of data to be transferred at high speed from one computer to another through the computers' data channel facilities.

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INTRODUCTION

The Multiprocessor Communications Adapter (MCA) facilitates the interconnection of up to fifteen Nova-line computers into a multiprocessor system by permitting blocks of data to be transferred at high speed from one computer to another through the computers' data channel facilities. Such a small-computer multiprocessor system is a powerful, highly flexible alternative to a single large computer in many applications.

APPLICATIONS

In situations characterized by relatively simple mathematical operations and substantial data communications and formatting requirements, a minicomputer multiprocessor system is often less expensive and far more flexible than any single medium to large-scale computer capable of meeting all the job requirements. Because several compatible processors are used, the system provides its own backup in case of failure.

In a typical multiprocessor system, one Nova-line computer might handle a number of data communication lines while another preprocesses data, and a third performs the actual computations. For example, a Nova 1200 Computer with multiple 4026/4027/4028 multiplexor systems can handle data communications multiplexing for at least 64 full duplex, teletype speed communications lines, freeing additional processors for editing, formatting, and concentration functions or for actual message processing. Such an approach is a more flexible, economic alternative to a dedicated hardware multiplexor for the control of multiple low speed lines.

In conjunction with a large-scale central processor, the minicomputer multiprocessor system described above might handle all data communications and formatting functions, as well as computations at a specified level of complexity, while message processing or store and foward operations were handled by the large-scale central processor.

The MCA is not required in systems with only modest intercommunication requirements. In such systems, a daisy chain interconnection of processors using the 4023 asynchronous interface is simpler and less expensive. Word transfer rates of up to 1KHz are practical without placing a high overhead burden on the system.

In systems with a shared data base, intercommunication through a shared fixed or moving head disk may obviate the need for the MCA. All Data General disk products offer the two processor feature.

OPERATION

One Multiprocessor Communications Adapter is attached to the IO bus of each computer in the system, and the adapters are connected together by a common communication bus which is time-division multiplexed among the adapters. Although mounted on a single circuit board, an adapter (MCA) actually contains independent receiver and transmitter subsections, allowing simultaneous reception and transmission of data. Each interface is connected separately to the data channel. The program need only set up an interface for receiving or sending and all transfers to and from memory are then handled automatically by the channel hardware. A processor with an adapter can establish a link between its transmitter and any receiver it designates, provided that the receiver adapter has been initialized for reception.

A number of logical links concurrently share the single communications bus using time partioning multiplexer circuitry built into the adapters. If there are N logical links established and communications is proceeding on all, each link receives 1/N of the communications bus time. The bandwidth of the bus is 500KHz (1 million bytes per second). However, this rate will only be obtained when a large number of links are active concurrently. Data rates are primarily determined by the processor's channel facilities. Typical data rates for a single link range from 70KHz for a pair of Novas to 140KHz for Nova-line computers with high speed data channel feature.

Since the receivers and transmitters are block transfer data channel devices, each contains a word-count, an address, and a status register. The word-count register is initialized to contain the twos complement of the number of words to be transferred; and the address register is initialized to contain the memory location of the first word transferred. The transmitter registers must be initialized by the transmitting processor; and the receiver registers must be initialized by the receiving processor. A transmitter can not force data into a receiving processor at addresses not specified by the receiver. Transmission of a block terminates with the shorter word count.

The MCA circuitry makes special provision for graceful degredation in the case of hardware and software failure. Not only is a receiving processor protected against a failing transmitter as described above, but the hardware is so arranged that any of the interconnected computers can be stopped or have their power switched off without affecting the other computers still in operation. If a processor adapter attempts to transmit data to an unavailable receiver adapter, a timeout interrupt will occur approximately 10 milliseconds (and several thousand attempts) later. If the receiver is unavailable because it is linked to another transmitter, the transmitter may be restarted for further attempts or the data may be routed to a different receiver.

Each adapter has a unique identifying number (between 1 and 15) assigned to it; these are established by jumpers in the adapter board as shown in Table 1. These codes are used to specify the number of a second adapter to which a first is to be logically connected. An IO instruction to the transmitter loads its status register with the code of the desired receiver. Upon receipt of the first data word from some transmitting adapter, the identifying number of the transmitter is set into the receiver adapter status register; the receiver will subsequently accept further data only from that transmitter, i.e., it "locks" to that transmitter. An IO instruction must be issued by the receiver processor to "unlock" the receiver adapter so that it can receive data from another transmitter.

The size and nature of the data transmission can follow any convention established by the user; no particular structure is forced by the hardware design. In a relatively simple system in which the size and nature of the data blocks to be transferred is always known in advance, the receiver can simply initialize itself to accept the next block at the completion of the previous transmission.

If the exact size and nature of the data blocks is determined dynamically, a control block specifying the nature of a transfer can be transmitted before the actual data block. With such a convention, the receiver initializes itself to accept a control block of standard format and unlocks itself. The first word transferred to the receiver locks it to the sending transmitter by setting the transmitter's code into its status register, locking it to that adapter transmitter until explicitly unlocked by the program. Thus, once the first word in a control block is received, the receiver is locked to that transmitter and can be initialized to accept subsequent data blocks from the appropriate transmitter.

Alternatively, the control block from adapter A to adapter B can be a request for data. Adapter B's transmitter can be started sending the desired data while its receiver is re-initialized to accept a new control block. The hardware in no way distinguish between data and control blocks.

IO INSTRUCTIONS

The multiprocessor communications adapter contains independent receiver (MCAR) and transmitter (MCAT) subsections. Both have their own status registers for control as well as independent word count, address, and data registers, following the standard Data General conventions.

For the receiver, BUSY and DONE are controlled or sensed by bits 8 and 9 in all IO instructions with device code 7, mnemonic MCAR. For the transmitter, BUSY and DONE are controlled or sensed by bits 8 and 9 in all IO instructions with device code 6, mnemonic MCAT. Interrupt disable is controlled by interrupt priority mask bit 12 for both.

RECEIVER

The MCA receiver sets DONE, clears BUSY, and interrupts the processor if:

a) The last word in a receiver's specified block is received (bit 15 of the receiver status register is set), or

b) The last word in a transmitter's specified block is received (bit 14 of the status register set) even if a longer block was specified by the receiver, or

c) The receiver timed out (bit 12 set).

The CLEAR function clears BUSY and DONE as well as bits 12 through 15 of the receiver status register; the receiver is disabled and unlocked. The START function clears DONE, clears bits 12, 14, and 15, and sets BUSY, enabling the receiver to accept data from a transmitter.

DIA - MCAR

DOA - MCAR

Read/load the receiver current address (CA) register from the selected accumulator. The register specifies the address of the next word to be stored into the processor's memory.

DIB - MCAR

DOB - MCAR

Read/load the receiver word count (WC) register from the selected accumulator with the twos complement of the number of words to be received. If read at the end of a transfer, the register contains the twos complement of the number of words remaining to be received.

DIC - MCAR

Read the receiver status register according to the format below. These bits are set in the adapter status register at the time DONE is set.

0-3 Code of the receiver as set by its jumpers.

4-7 When locked, the code of the transmitter to which the receiver is logically connected. The transfer of a single word to a receiver sets these bits in the receiver status register to the code of the sending transmitter and makes the receiver go locked, insuring that it will accept no data from any other transmitter.

8-11 Unused

12 Timeout: Data transmission has been in progress, but no new data has been sent in the last 10 milliseconds. This usually means that a hardware failure has occurred or power is off in the transmitter's processor. This timeout does not occur if the transmitter word count goes to zero which indicates a shorter block length than the receiver's.

13 Locked: The receiver has begun accepting data from a transmitter.

14 Transmitter has sent the last word of a block as specified by its WC.

15 Receiver WC went to zero indicating that the transfer specified by the receiver has been completed.

Revision 03 (and later) MCA's can be used with the standard program load/channel start option. Channel start to the MCAR enables it to accept a data block into memory locations 0 - 377 (octal) from some transmitter's adapter, just as it would from disk or magnetic tape.

TRANSMITTER

The MCA transmitter sets DONE, clears BUSY, and interrupts the processor if:

a) The last word permitted by the receiver is sent (bit 15 of the transmitter's status register is set),

b) The last word in a transmitter specified block is sent (bit 14), or

c) The transmitter timed out (bit 12).

The CLEAR function clears the BUSY and DONE in the transmitter's status word. When BUSY is cleared transmission is immediately stopped. If transmission were in progress when the CLEAR function occurred, a word might be lost. The START function clears DONE and sets BUSY, initiating the block transfer specified by the transmitter CA, WC and status registers.

DIA - MCAT

DOA - MCAT

Read/load the transmitter current address (CA) register from the selected accumulator. The register specifies the address of the next word to be stored into the processor's memory.

DIB - MCAT

DOB - MCAT

Read/load the transmitter word count (WC) register from the selected accumulator with the twos complement of the number of words to be transmitted. If read at the end of a transfer, the register contains the twos complement of the number of words remaining to be transmitted.

DIC - MCAT

DOC - MCAT

Read/load the transmitter status register according to the following format. Note that only bits 0-3 may be changed with a DOC instruction and that bits 12-15 are valid only when DONE is set.

0-3 Code of the receiver desired (1-15).

4-7 Code of the transmitter as set by its jumpers.

8-9 Unused

10-11 Used for diagnostic mode only; must be 0 during DOC.

12 Timeout: Data transmission has been attempted but the selected receiver has not acknowledged within the last 10 milliseconds. This means either that power is off in the selected receiver's processor (or some other hardware failure has occurred) or that it is locked to another transmitter. The timeout does not occur if the receiver word count goes to zero during transmission as this merely indicates a shorter block length than that specified at the transmitter.

13 Locked: The designated receiver is locked to some transmitter.

14 The transmitter word count went to zero indicating that the block transmission has been completed.

15 The receiver word count went to zero. If desired, the transmission may be continued using a NIOS instruction as the 3 registers are set with the proper control data.

The transmitter interrupt service routine is the most complex part of MCA programming. The general flow of the MCAT service routine is as follows:

1) The DIC AC, MCAT instruction is used to read the status of the adapter transmitter. Approximately 6 microseconds should be allowed to elapse between detection of the MCAT DONE flag and the DIC instruction. This delay is usually inherent in the interrupt service routine entry procedure.

2) The receiver and transmitter count done bits (14, 15) should be tested first. If either is set, the appropriate count done handler part of the service routine can be entered.

3) If bits 14 and 15 are not set, the time out bit (13) is presumeably set. The DIB AC, MCAT instruction is issued to determine the number of words, if any, which have been transmitted. If more than one word has been transmitted, the desired receiver has had a hardware failure during transmission of the data block. If no words or one word has been transmitted, either there is a hardware failure or the receiver is legitimately unable to accept data at that time. The receiver adapter might not be enabled or it might be locked to another transmitter. The transmitter program should make several more attempts to transmit the data block. The transmitter should be restarted using the NIOS MCAT instruction so that the WC, CA, and Status registers are not altered.

DIAGNOSTIC MODE

The MCA includes a special diagnostic mode which facilitates maintenance. This mode is entered if bit 11 of the selected accumulator is set during the DOC AC, MCAT instruction. the DIC AC, MCAT instruction reads back the diagnostic mode status in bit 11 and the bus phase in bit 10 (1 = status phase, 0 = data phase). When the MCA is in diagnostic mode, the diagnostic program can step the hardware through its various clock phases using the NIOP MCAT instruction.

The MCA under test must be disconnected from the communications bus to run the diagnostic test #095-000661. Any number of MCA's are tested as an interconnected system using reliability test #095-000062.

INSTALLATION

The Multiprocessor Communications Adapter is a direct memory access data channel device which mounts on a standard Data General 15-inch square printed circuit board. It plugs directly into one of the subassembly slots in a Nova-line chassis and is capable of using the high speed channel feature, if the processor is so configured. Two 50 pin cannon connectors interface the adapter to the common communications bus. The IN connector of one adapter is cabled to the OUT connector of the next in a daisy chain.

Each adapter contains a terminator network for the communication bus. In a system containing two adapters, the terminator networks operate as supplied. In systems containing more than two adapters, the terminators must be removed from all adapters except those at the ends of the communications bus. To do this, the user removes all 270 ohm resistors from the middle adapters and replaces all 180 and 220 ohm resistors with 10K ohm resistors. If an additional adapter is added to either end of an installed system, the terminators must be removed from the existing adapter as individual adapters are shipped with terminators in place.

Each adapter contains four jumpers that are set by the user to assign a code to the receiver/transmitter pair. When a system is configured, the jumpers are installed to establish sequential addresses beginning with one (1). Table 1 shows the jumper pattern for various codes.

The data rate of the communications bus can be reduced if necessary to permit additional cable lengths. The 500KHz word transfer rate is supplied as standard, but it may be reduced to 300KHz in order to lengthen the maximum bus length to 90 feet from the standard 40 feet. Install jumper W5 in every adapter to establish the lower speed.

In large configurations, an independent second MCA system can be installed. Device codes 46 and 47 are used for the second system, established by removing jumper W6 and installing W7 on all adapters connected to the second system. An MCA, using the alternate device codes, can be installed as the second adapter on a particular processor/communications bus if it is desired to increase the data transfer rate through that processor.

TABLE 1

ADAPTER CODE	JUMPERS INSTALLED
0	Not Used
1	Wl
2	W3
3	Wl, W3
4	W2
5	Wl, W2
6	W2, W3
7	Wl, W2, W3
8	W4
9	Wl, W4
10	W3, W4
11	Wl, W3, W4
12	W2, W4
13	Wl, W2, W4
14	W2, W3, W4
15	Wl, W2, W3, W4