[10] S. M. M. S. M. M. S. M								
			TRANSMIT	TER				
D								
	8X CLK							
			[]					
	DIV8 B	I						
		DC)B					
		THE DOA SETS TI=I AND LO	ADS THE DATA TO BE TRANSMITTED I	NTO THE YMITTER BURFER				
	TI	SHIFTER IS LOADED WITH TH	E CHARACTER TO BE XMITTED TO TH	E LEFT OF THE CHARACTER I	N THE SHIFTER ARE LOR 2 S			
		IN THE SHIFTER. TO THE	LEFT OF THE STOP BITS ALL BIT PLAC	ES IN THE SHIFTER = I. ALL	SHIFTS INTO THE SHIFTER P	ROM THE LEFT = 1.		
	BUSY							
(STATE OF THE FLIP-F THE RIGHT OF XMITTER	LOP TO							
THE RIGHT OF AMILTER	JUFFER	[]	DOB CLEARS XMITTER DONE		<u> </u>			
XMITTER DO	NE SET]	DOB CLEARS ANTITER DONE					
SHIFT		THE RIGHT-MOS	T SHIETED BUT					
		PLACE IS THE OUT PUT LINE. MOVES THE NEI TRANSMITTED IN TO THE	SIT ON THE SERIAL EACH SHIFT ENABLE T BIT TO BE DIGHT-MCST PLACE					
SHIFTER	EMPTY						х -	
	THE SHIFTER IS EMP	TY IF ALL BITS IN THE SHIFTER - I EXCEP OADED) IS ON THE LINE ON THE NEXT	THE RIGHT-MOST. THEREFORE THE SI 8x CLK, BUSY IS CLEARED.	IFTER IS EMPTY WHEN THE LAS	T STOP BIT (WHICH WAS THE	LEFT-MOST Ø WHEN		
			RECEIVER					و
TI CLOCK GENE (AND SPIKE DECTOR) SHIFT E		SIGNAL IS GENERATED ONCE EVERY EI NORE BIT FROM THE SERIAL INPUT (RE	SHT BX CLKS. EACH TI CLOCK SHIFTS CEIVED DATA).		ER ONE PLACE RIGHT AND			
TI CLOCK GENE (AND SPIKE DECTOR) SHIFT E	RATOR NABLE AT THIS TIME THE STAI BIT IS DETECTED	SIGNAL IS GENERATED ONCE EVERY EI KORE BIT FROM THE SERIAL INPUT (RE IF, WHEN THE RECEIVER IS IDL SERIAL INPUT LINE IS AT LEA	SHT & CLKS. EACH TI CLOCK SHIFTS CEIVED DATA). E. A SPACE ON THE ST FOUR & CLK TIMES	THE CONTENTS OF THE TI BUFF				
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UNLESS OTHERWISE SPECIFIED- DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± XX ± PARTS TO BE FREE FROM BURGS BRARA ALL EDGES JOID	ENGINEER	s/72			RAL CORPOI	
PARTS TO BE FREE FROM BURRS						
	APPROVED	NOTES & WAVE FORMS				
UNLESS OTHERWISE SPECIFIED . ALL MACH. SURFACES MATERIAL	FIRST USED ON		Ν	NCD, 4	060 SER	IES
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