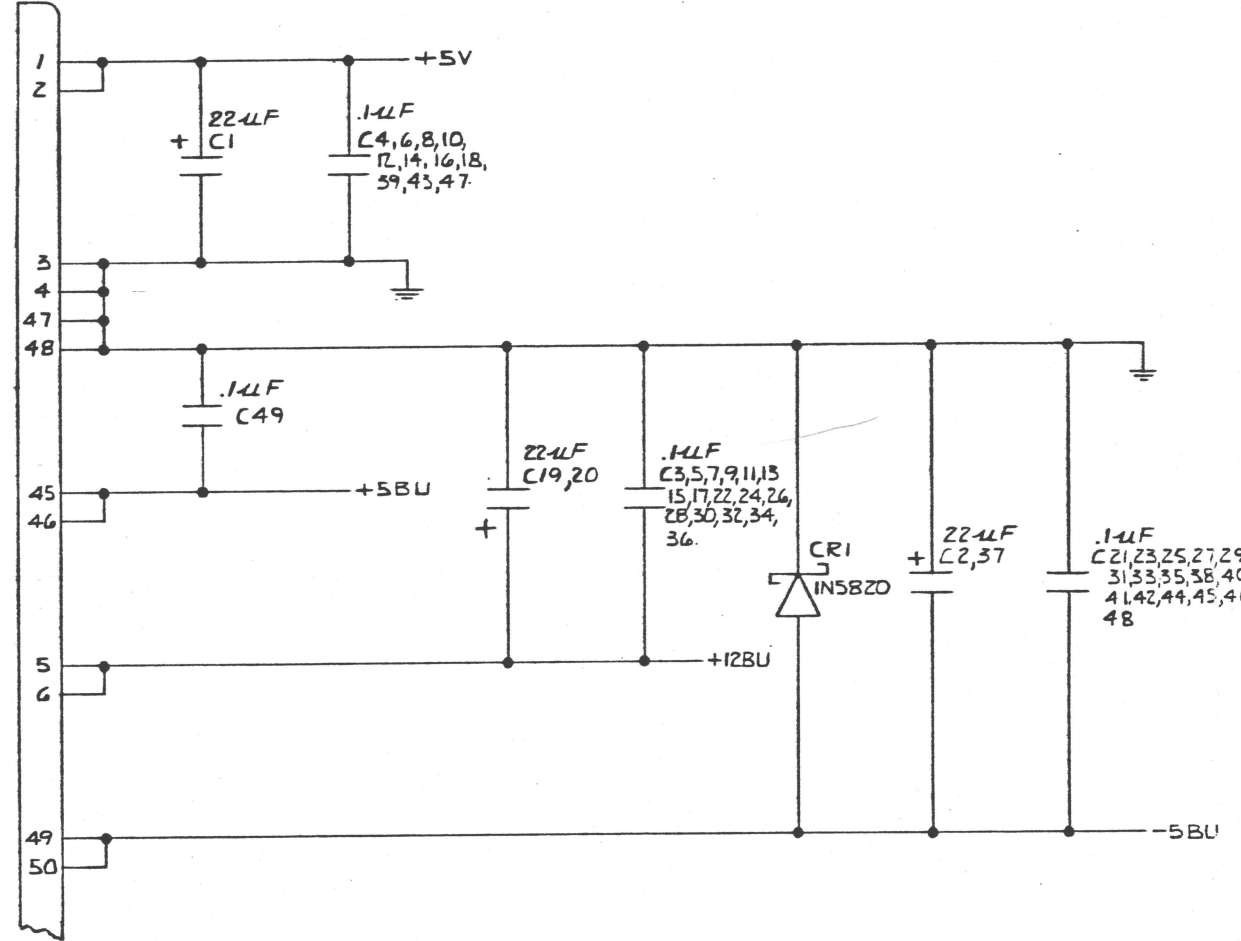


REVISIONS				
PART REV.	DOC REV.	DESCRIPTIONS	DATE	APPROVED
A	A	INITIAL PRODUCTION RELEASE	12-2-81	FV

J3 EDGE CONNECTOR

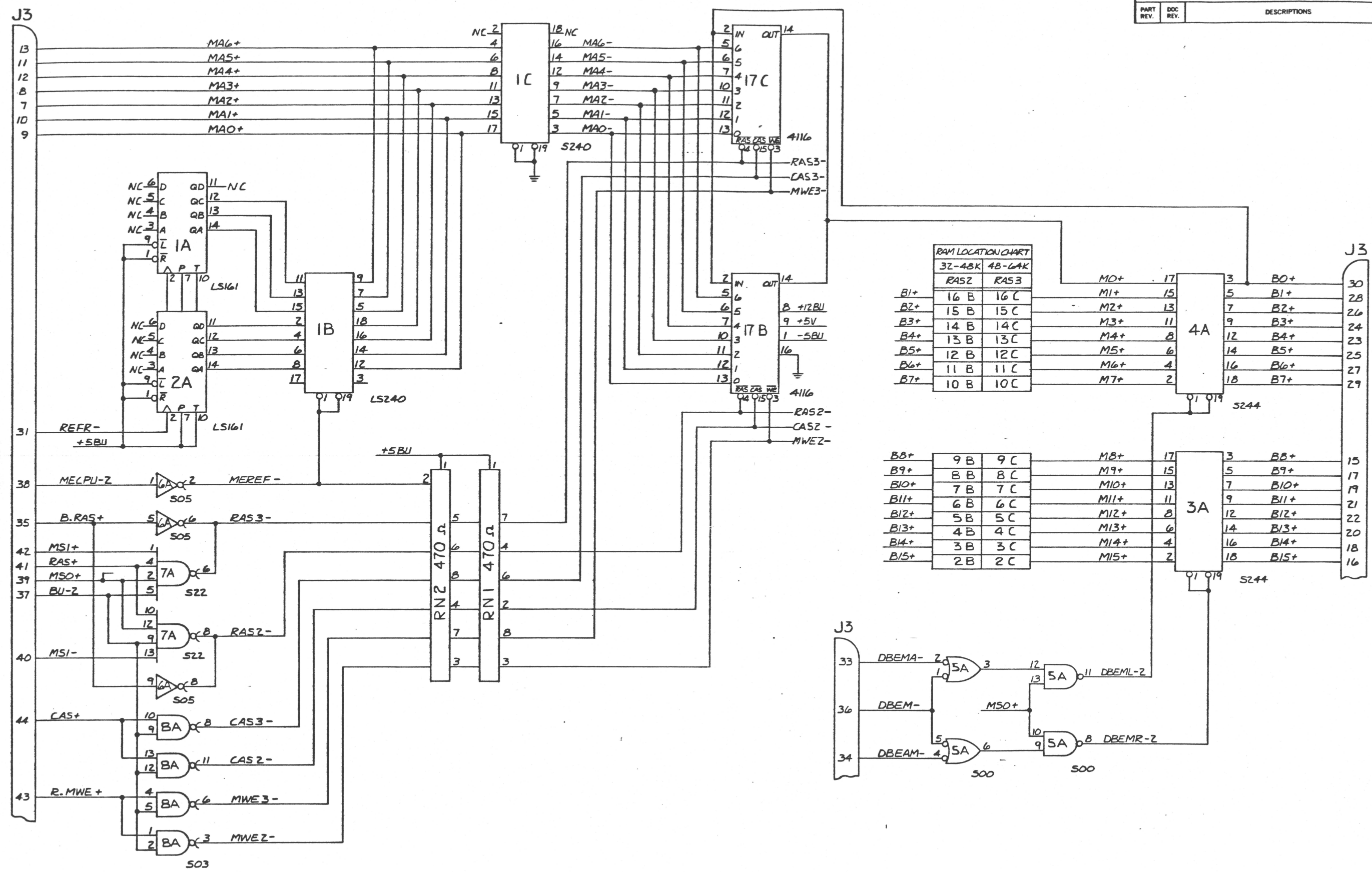


UNUSED GATES			
REF	TYPE	PIN NUMBER	
		IN	OUT
6A	74505	3,11,13	4,10,12
1C	745240	2	18
1B	74LS240	17	3

- 6. LAST USED REF. DESIGNATORS.
- C. CAPACITOR - C49
- B. DIODE - CR1
- L. RES. S/P - RN2
- 5. ALL CAPACITOR VALUES ARE IN PICOFARADS.
- 4. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
- 3. FOR PARTS LIST SEE DWG. NO. 20102
- 2. FOR ASSY SEE DWG. NO. 20103
- 1. FOR P.C. BOARD DETAIL SEE DWG. NO. 20100

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS .XX ± DECIMALS .XXX ± ANGLES ±		POINT DATA CORPORATION Irvine, California 92714	
APPROVALS DRAWN: J. MASCHHAUPT CHECKED: JDE BARALYA PRODUCTION: <i>[Signature]</i>		DATE 11-25-81 11-25-81	
SIZE: D NEXT ASSEMBLY: 20103 DRAWING NO.: 20104		SCHEMATIC DIAGRAM CPU PIGGYBACK MARK 3 (EXTENDED MEMORY)	
THIS DRAWING AND THE INFORMATION CONTAINED HEREON ARE PROPRIETARY TO POINT 4 DATA CORPORATION AND SHALL NOT BE REPRODUCED, COPIED, USED OR DISCLOSED TO OTHERS WITHOUT THE PRIOR WRITTEN CONSENT OF POINT 4 DATA CORPORATION.		SCALE: DO NOT SCALE DRAWING	SHEET 1 OF 5



NOTES: UNLESS OTHERWISE SPECIFIED

J3		
TOP	SIGNAL	DIRECT
1	+5V	IN
3	GND	IN
5	+12BU	IN
7	MA2+	IN
9	MA0+	IN
11	MA5+	IN
13	MAG+	IN
15	B8+	BI
17	B9+	BI
19	B10+	BI
21	B11+	BI
23	B4+	BI
25	B5+	BI
27	B6+	BI
29	B7+	BI
31	REFR-	IN
33	DBEMA-	IN
35	B.RAS+	IN
37	BU-2	IN
39	MS0+	IN
41	RAS+	IN
43	R.MWE+	IN
45	+5BU	IN
47	GND	IN
49	-5BU	IN

J3A		
TOP	SIGNAL	DIRECT
1	+5V	IN
3	GND	IN
5	+12BU	IN
7	MA2+	IN
9	MA0+	IN
11	MA5+	IN
13	MAG+	IN
15	B8+	BI
17	B9+	BI
19	B10+	BI
21	B11+	BI
23	B4+	BI
25	B5+	BI
27	B6+	BI
29	B7+	BI
31	REFR-	IN
33	DBEMA-	IN
35	B.RAS+	IN
37	BU-2	IN
39	MS0+	IN
41	RAS+	IN
43	R.MWE+	IN
45	+5BU	IN
47	GND	IN
49	-5BU	IN

D
C
B
A

NOTES: UNLESS OTHERWISE SPECIFIED