Publications Update

MARK 386S Business System Installation/ Operation Guide

Incorporation of the attached pages into Revision A of the manual brings it up to Revision B

November 1990

Publications Update

TO: MARK 386S Users

FROM: Publications Department

DATE: November 29, 1990

SUBJ: MARK 386S INSTALLATION/OPERATION GUIDE, REVISION B UPDATE PACKAGE

The MARK 386S Installation/Operation Guide has been updated. The revised pages are attached. Incorporation of these pages into a Revision A document brings it up to Revision B. Remove and insert pages as indicated below.

FILING INSTRUCTIONS

Remove	Insert
Title thru vii	Title thru ix
2-19/2-20	2-19/2-20
4-11/4-12 4-15	4-11/4-12 4-15 thru 4-18
none	D-1 thru D-11
none	E-1 thru E-8
Comment Sheet/Mailer	Comment Sheet/Mailer

MARK 386S

BUSINESS SYSTEM INSTALLATION/ OPERATION GUIDE

Revision B

NOTICE

Every effort has been made to make this manual complete, accurate and up-to-date. However, all information herein is subject to change due to updates. All inquiries concerning this manual should be directed to POINT 4 Data Corporation.

WARNING!

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Document Order Number: HTP0091

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REVISION RECORD

PUBLICATION NUMBER: HM-240-0091

Revision	Description	Date
A	Initial Customer Release	04/20/90
B	Update including new Appendices D and E; changes to Section 4	11/29/90

LIST OF EFFECTIVE PAGES

Changes, additions, and deletions to information in this manual are indicated by vertical bars in the margins or by a dot near the page number if the entire page is affected. A vertical bar by the page number indicates pagination rather than content has changed. The effective revision for each page is shown below.

Page	Rev	Page	Rev	Page	Rev
Cover	-				
Title thru ix	B				
1-1 thru 1-10	A				
2-1 thru 2-18	A				
2-19	B				
2-20 thru 2-23	A				
3-1 thru 3-12	A				
4-1 thru 4-10	A				
4-11	B				
4-12 thru 4-15	A				
4-16 thru 4-18	B				
5-1 thru 5-3	A				
6-1 thru 6-4	A				
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A-1 thru A-3	A				
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E-1 thru E-8	B				
Comment Sheet	B				
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CONTENTS

SECTION 1. GETTING TO KNOW YOUR COMPUTER

SECTION 2. INSTALLING INTERNAL OPTIONS

APPENDICES

FIGURES

TABLES

2.7 INSTALLING THE 8-PORT SERIAL CONTROLLER

Instructions for installing the 8-port Serial Controller are contained in the *8-Port Serial Controller User Guide*, dated November 1988 (Order Number HTP0076).

Using the Arnet driver, XENIX supports a maximum of two 8-port controllers, one as COM1 and the other as COM2. XENIX does not support chaining two or more boards on one interrupt.

2.7.1 Installing the 8-Port Serial Controller as COM1

1. JP1 must have a jumper across location 3.
2. JP2 must have a jumper across location 3 (IRQ4).
3. Set SW1, keys 1 through 4, to 1 0 1 1, where 1=ON or Closed (Address 100H).
4. Set SW2, keys 1 through 8 to 1 0 1 0 1 1 0 0.
5. On the 1P/2S Adapter change Port 1 to use COM3 instead of COM1 (see Table 2-8).
6. Run **mkdev serial** to install an 8-port card on COM1.

2.7.2 Installing a Second 8-Port Serial Controller as COM2

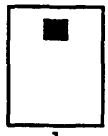
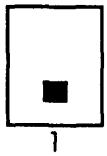
1. JP1 must have a jumper across location 3.
2. JP2 must have a jumper across location 2 (IRQ3).
3. Set SW1, keys 1 through 4, to 1 0 0 1, where 1=ON or Closed (Address 180H).
4. Set SW2, keys 1 through 8, to 1 0 0 0 1 1 0 0.
5. On the 1P/2S Adapter change Port 2 to use COM4 instead of COM2 (see Table 2-8).
6. Run **mkdev serial** to install an 8-port card on COM2.

2.8 INSTALLING THE ATI VIDEO ADAPTER

There are four switches in one assembly on the rear of the card.

Switch 1 (SW1) is used to select the mode of operation which will be in effect at power-on (see Table 2-4).

Table 2-4. Video Mode Select

Default Mode	Graphics Solution SW1 Switch Settings
Color/Graphics	 OFF/Closed ON/Open
Monochrome/Graphics	 OFF/Closed ON/Open
Color/Graphics – Selects for IBM Color/Graphics, Plantronics Color/Graphics and ATI 640 x 200 16 Color/Graphic modes. **Monochrome/Graphics** – Selects for Monochrome Text Mode (MDA), and Hercules Monochrome/Graphics Mode.	

Switches 2 and 3 are used to identify the type of monitor that is being used (see Table 2-5).

Table 4-3. MAXTOR 765MB, FAB #7 Jumper Settings (Continued)

PCBA: 1014150 10
TLA #: 1098068 2
FAB #: 7

JUMPER ADDRESS	STATUS MK 386S	DESCRIPTION
JP31	Out	Hard/Soft Sector Mode; In=Soft Sector
JP32	In	Head Select Jumpers
JP33	In	Head Select Jumpers
JP34	In	Head Select Jumpers
JP35	In	Head Select Jumpers
JP36	Out	Head Select Jumper
JP37	Out	PLO Sync Field Lengths
JP38	Out	NOT USED
JP39	Out	NOT USED
JP40	Out	Factory Selected
JP41	Out	Test Pins Differential Data Signals
JP42	In (B-C)	Test Pin - Write Gate to Flex Circuit
JP43	In	Test Out Disables On-board RAM
DS1	In	DRIVE SELECT
DS2	Out	DRIVE SELECT
DS3	Out	DRIVE SELECT
DS4	Out	DRIVE SELECT
DS5	Out	DRIVE SELECT
DS6	Out	DRIVE SELECT
DS7	Out	DRIVE SELECT

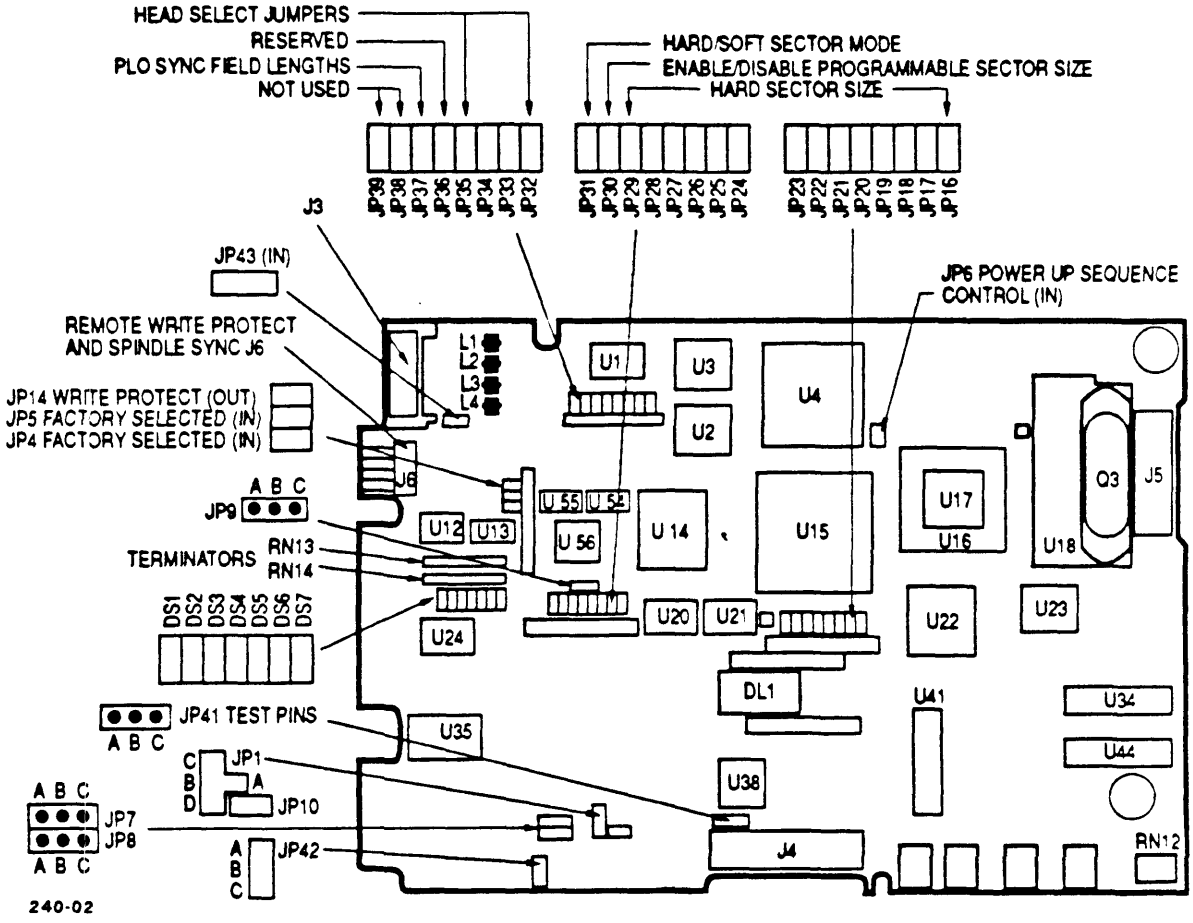


Figure 4-1. MAXTOR PCBA #1014520, FAB #9

MS-DOS then asks:

Format another? (Y/N)

Type "N" to stop the format process.

Table 4-4. MAXTOR 765MB Jumper Settings

PCBA: 1023856 1
TLA #: N/A
FAB #: N/A

JUMPER ADDRESS	STATUS MK 386S	DESCRIPTION
JP1	A-B	Encoded Write Data
JP2	N/A	
JP3	N/A	
JP4	Out	Out=1,7 Encoding
JP5	In	In=15Mbit/sec Transfer Rate (Hard Wired)
JP6	In	In=Motor Remote Spinup Option Disabled Out=Motor Spinup Option Enabled
JP7	B-C	Read Gate Delay Option
JP8	Out	Read Gate Delay Option
JP9	A-B	INDEX Width Selection. A-B=2.8µsec. B-C=70µsec.
JP10	In	Write Current Select (Hard Wired)
JP11	N/A	
JP12	N/A	
JP13	N/A	
JP14	Out	In=Write Protect
JP15	N/A	
JP16	Out	Hard Sector Size
JP17	Out	Hard Sector Size
JP18	In	Hard Sector Size
JP19	In	Hard Sector Size
JP20	In	Hard Sector Size
JP21	Out	Hard Sector Size
JP22	In	Hard Sector Size
JP23	Out	Hard Sector Size
JP24	Out	Hard Sector Size
JP25	In	Hard Sector Size
JP26	Out	Hard Sector Size
JP27	Out	Hard Sector Size
JP28	Out	Hard Sector Size
JP29	Out	Hard Sector Size
JP30	Out	Out=Disable ESDI Programmable Sector Size (Hard Sector Mode Only) In=Enable ESDI Programmable Sector Size (Hard Sector Mode Only)

Table 4-4. MAXTOR 765MB Jumper Settings (Continued)

PCBA: 1023856 1
TLA #: N/A
FAB #: N/A

JUMPER ADDRESS	STATUS MK 386S	DESCRIPTION
JP31	Out	In=Soft Sector Mode;Out=Hard Sector Mode
JP32	In	Drive Model Selection
JP33	In	Drive Model Selection
JP34	In	Drive Model Selection
JP35	In	Model Select 0
JP36	Out	Reserved
JP37	In	Bytes per PLO Sync Field
JP38	Out	Model Select 1
JP39	In	Bytes per PLO Sync Field
JP40		Test Jumper
JP41	Out	Test Pins (Differential Data Read Signals)
JP42	B-C	Write Enable Select
JP43	In	Test Out Disables On-board RAM
DS1	In	DRIVE SELECT
DS2	Out	DRIVE SELECT
DS3	Out	DRIVE SELECT
DS4	Out	DRIVE SELECT
DS5	Out	DRIVE SELECT
DS6	Out	DRIVE SELECT
DS7	Out	DRIVE SELECT

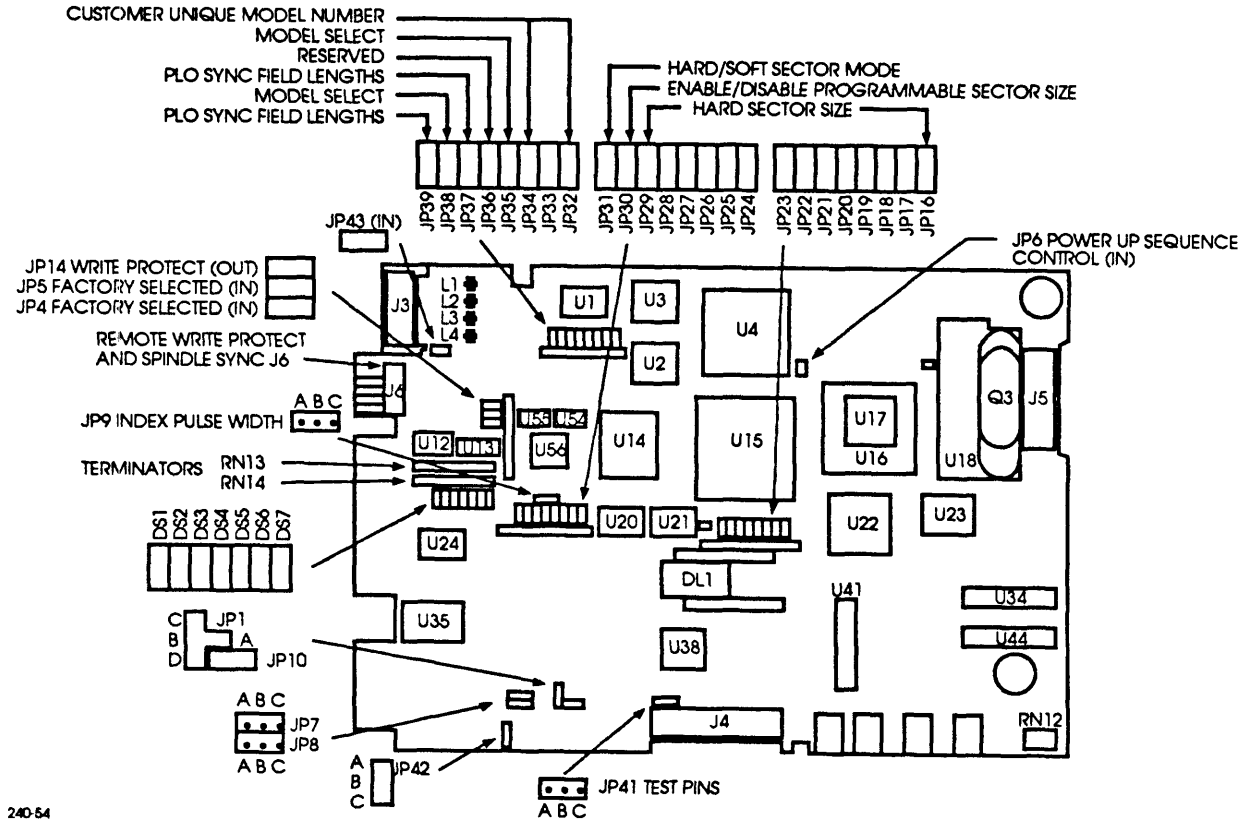


Figure 4-4. MAXTOR PCBA #1023856 1

Appendix D
80386DX-33 MOTHERBOARD CONFIGURATION

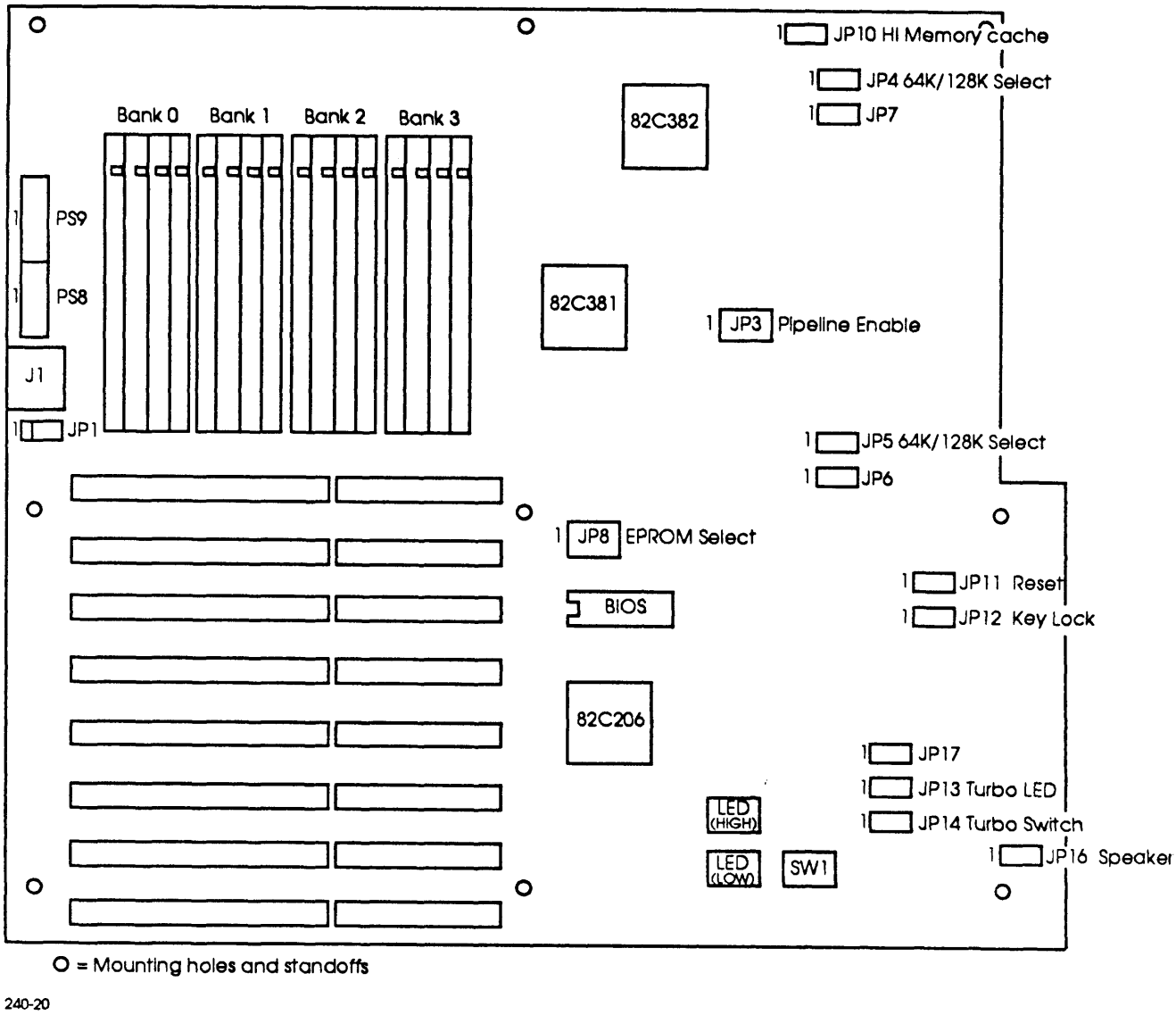


Figure D-1. 80386DX-33 Motherboard Layout

Table D-1. 80386DX-33 Jumpers and Switch Settings

PS8 and PS9	Power Connectors Plug In with Black Wires Together		
J1	Keyboard Connector		
JP1	Battery Connector (Red is Pin 1)		
JP3	Pipeline Select 1-2 turns OFF pipeline 2-3 turns ON pipeline Default is "OFF" with cache Default is "ON" without cache		
JP4 to JP7	64K/128K Cache Select 1-2 selects 128K 2-3 selects 64K		
JP8	EPROM Select 1-2 selects 512K EPROM 2-3 selects 256K EPROM Default is 512K		
JP10	High Memory Cache/Noncache 1-2 High Memory Noncacheable 2-3 High Memory Cacheable (default)		
JP11	RESET Connector		
JP12	Keylock Connector		
JP13	TURBO LED Connector		
JP14	TURBO Switch Connector		
JP16	Speaker Connector		
JP17	Emergency 206 RESET		
SW1	DIP Switch		
	1		"ON" for color "OFF" for mono
	2	3	
	ON	OFF	Speed change by keyboard (CTRL/ALT/+ for high speed, CTRL/ALT/– for low speed). (Also set CPU = CLKIN in setup – see Figure D-5B.)
	OFF	ON	Speed change by TURBO Switch (Also set CPU = ICLK in setup – see Figure D-5B.)

CMOS SETUP © Copyright 1985-1989, American Megatrends, Inc.

```
Date (mn/date/year) : Sun, Jan 01 1989
Time (hour/min/sec) : 00:42:53
Floppy drive A      : 1.2MB, 5-1/2"
Floppy drive B      : Not Installed

Hard disk C:type    : 1
Hard disk D:type    : Not Installed
Primary display     : Monochrome
Keyboard            : Installed

Scratch RAM option  : 1

Month  : Jan, Feb, ... Dec
Date   : 01, 02, 03, ... 31
Year   : 1901, 1902, ... 2099
```

```
Base memory size  : 640KB
Ext. memory size  : 0KB
Numeric processor : Installed
```

Cyln	Head	WPcom	LZone	Sec	Size
615	4	300	615	17	20MB

Sun	Mon	Tue	Wed	Thu	Fri	Sat
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31	1	2	3	4
5	6	7	8	9	10	11

ESC=Exit,<>=Select,PgUp/PgDn=Modify

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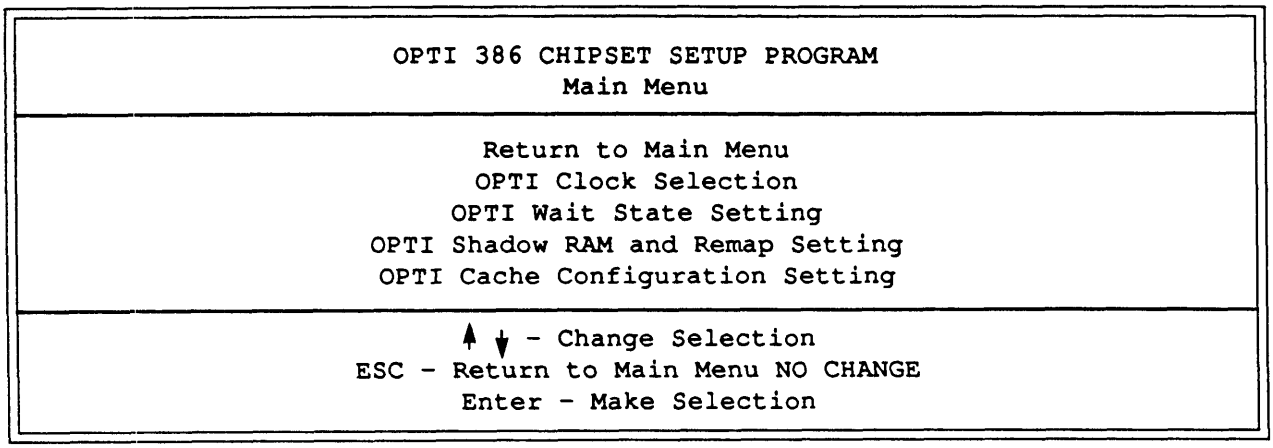
Figure D-2. 80386DX-33 CMOS SETUP Screen

OPTI 386/486 CHIPSET SETUP PROGRAM
Main Menu

Easy Setup OPTI Chipset
Advanced Setup OPTI Chipset
Write CMOS Registers and Exit
Do Not Write CMOS Registers and Exit

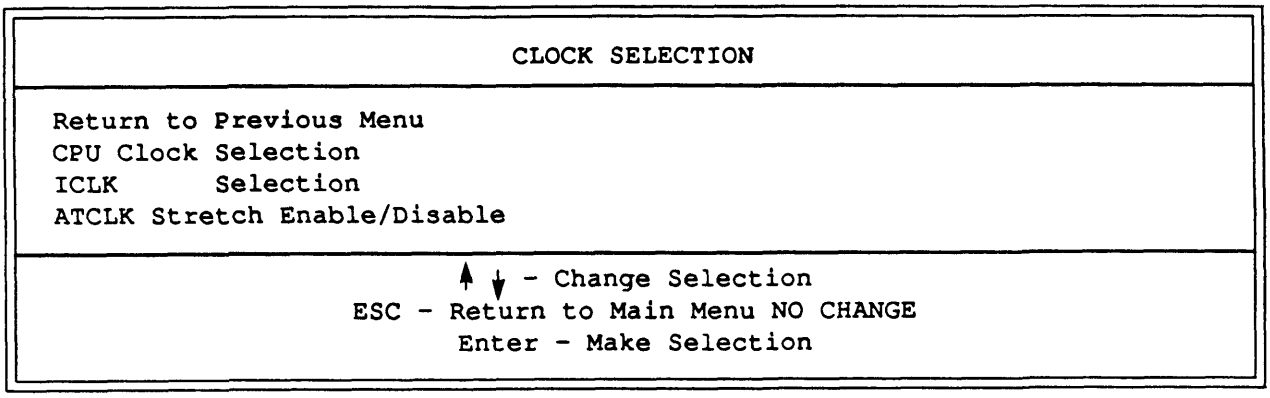
240-22

Figure D-3. XCMOS SETUP SCREEN



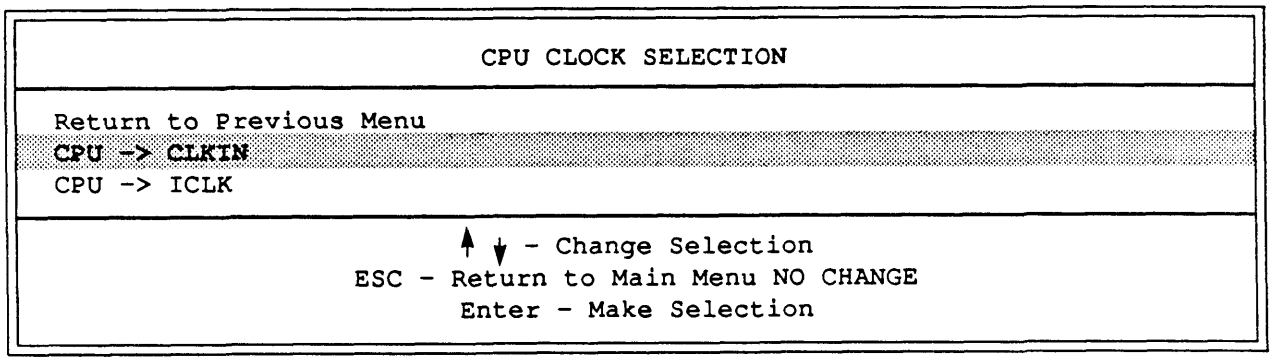
240-23

Figure D-4. EASY SETUP OPTI CHIPSET



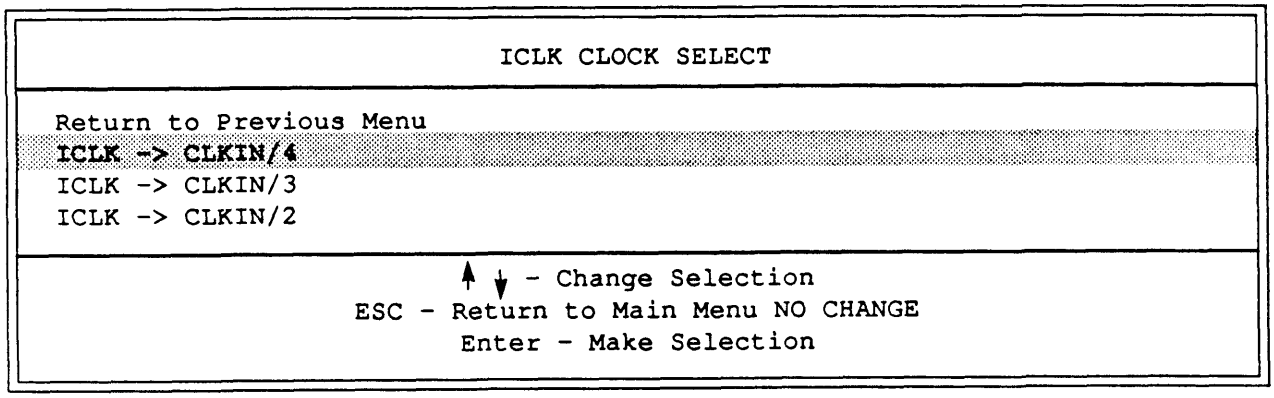
240-24

Figure D-5. OPTI Clock Selection



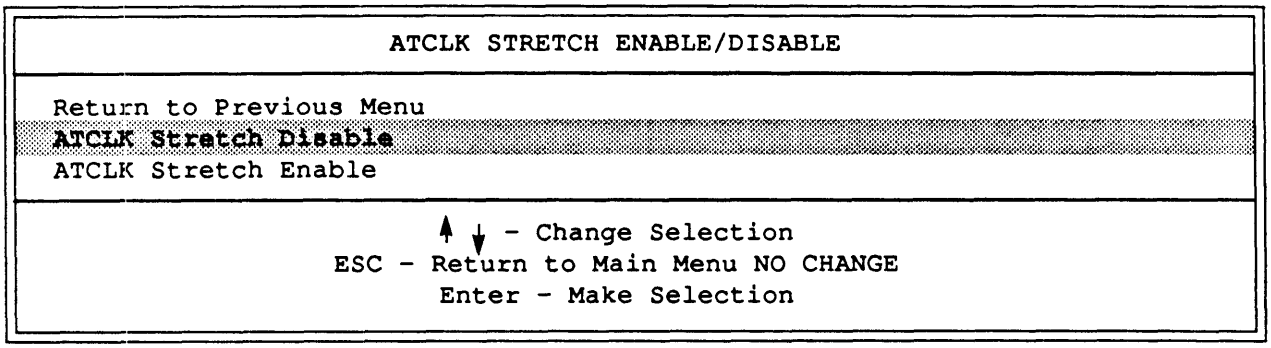
240-25

Figure D-5A. CPU Clock Selection



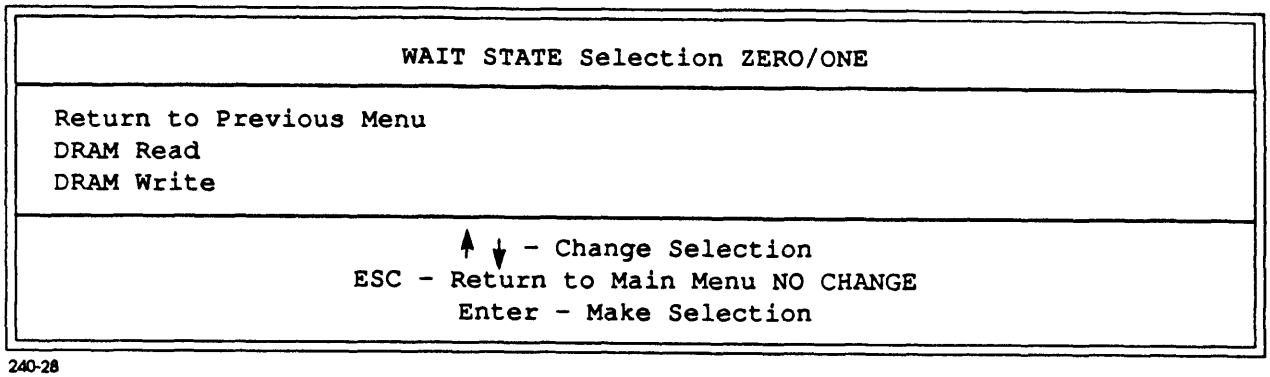
240-26

Figure D-5B. ICLK Selection



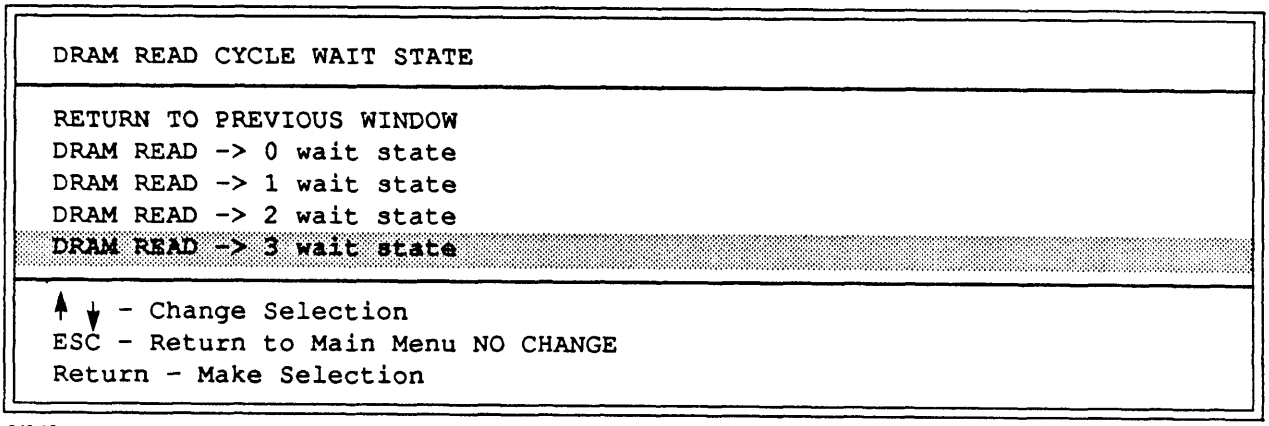
240-27

Figure D-5C. ATCLK Stretch Enable/Disable



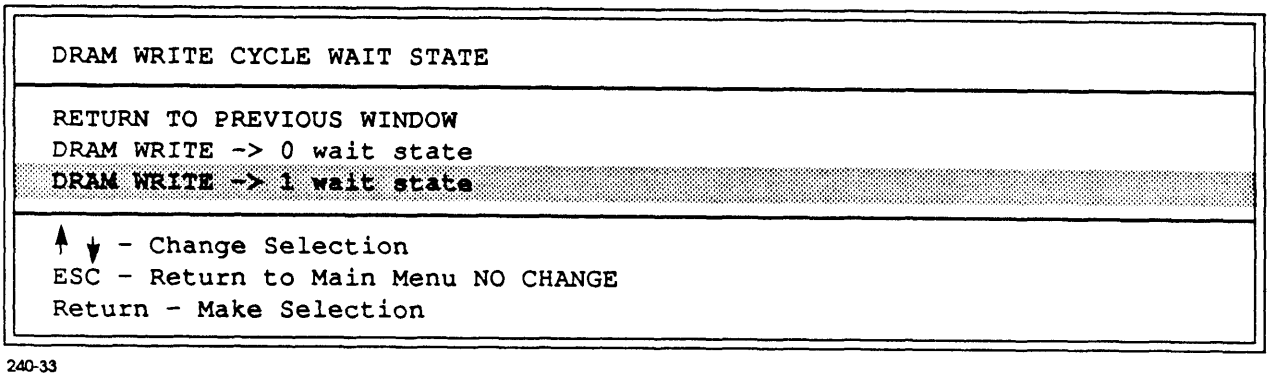
240-28

Figure D-6. OPTI Wait State Setting



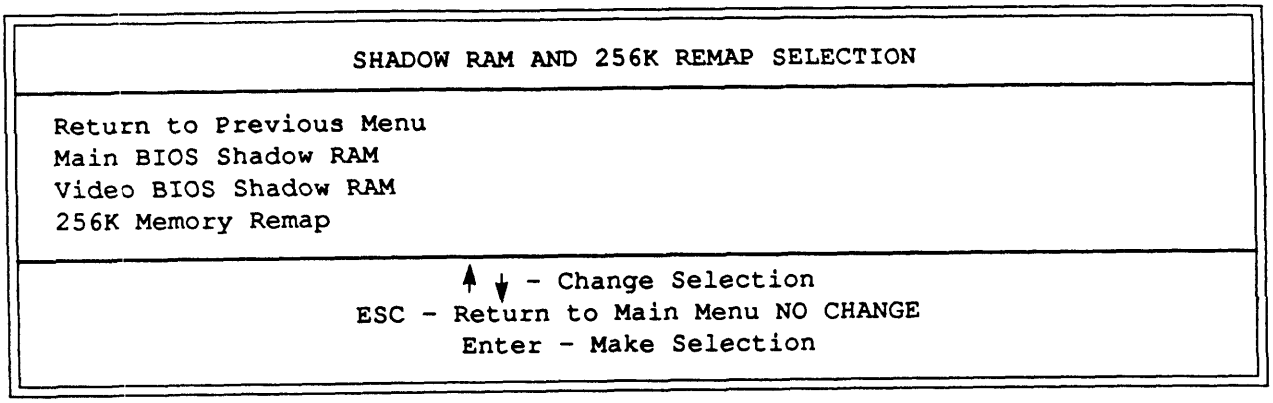
240-32

Figure D-6A. DRAM READ Cycle Wait State



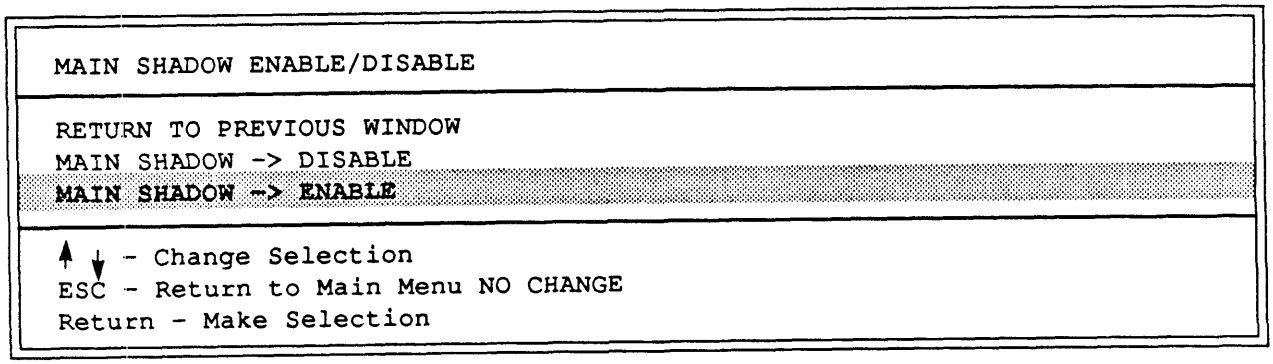
240-33

Figure D-6B. DRAM WRITE Cycle Wait State



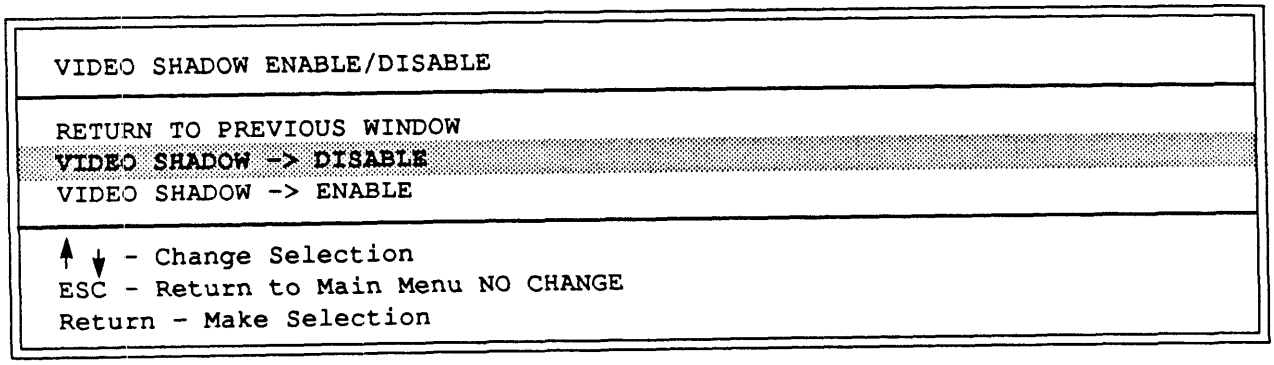
240-29

Figure D-7. OPTI Shadow RAM and REMAP Setting



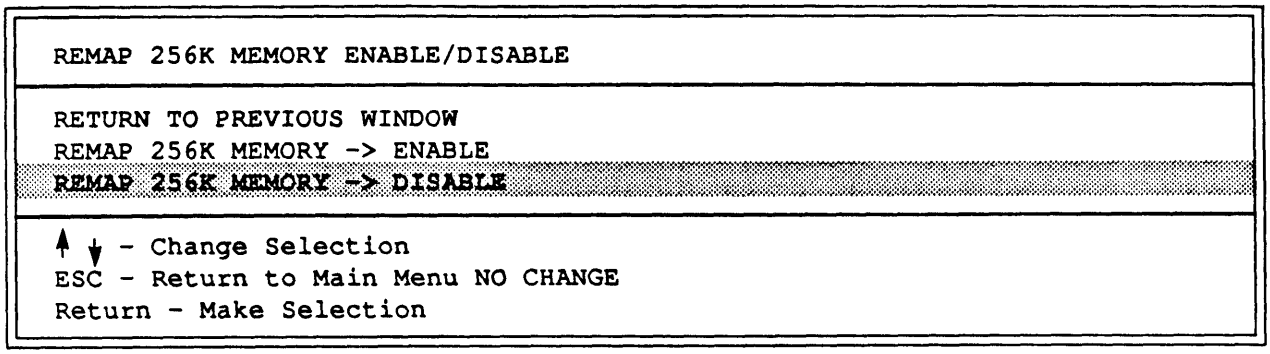
240-34

Figure D-7A. Main Shadow ENABLE/DISABLE



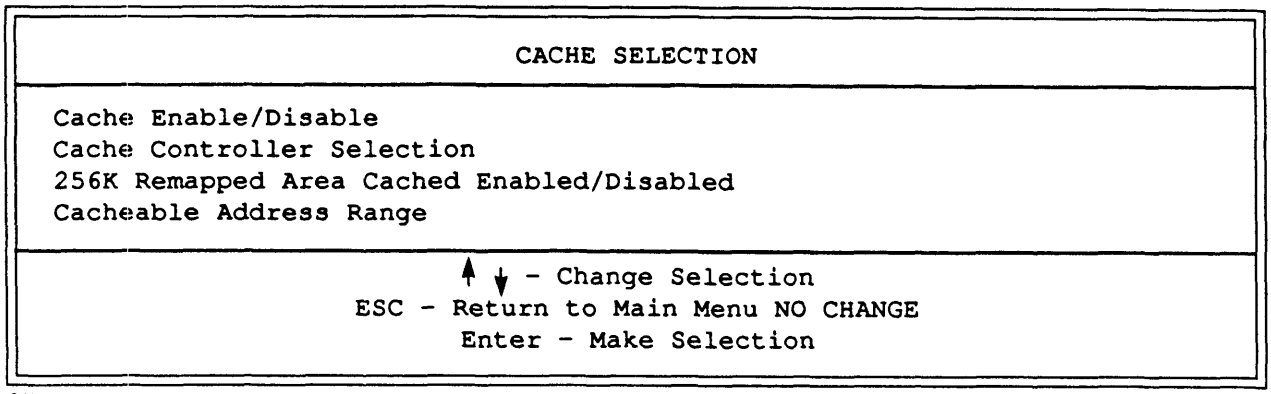
240-35

Figure D-7B. Video Shadow ENABLE/DISABLE



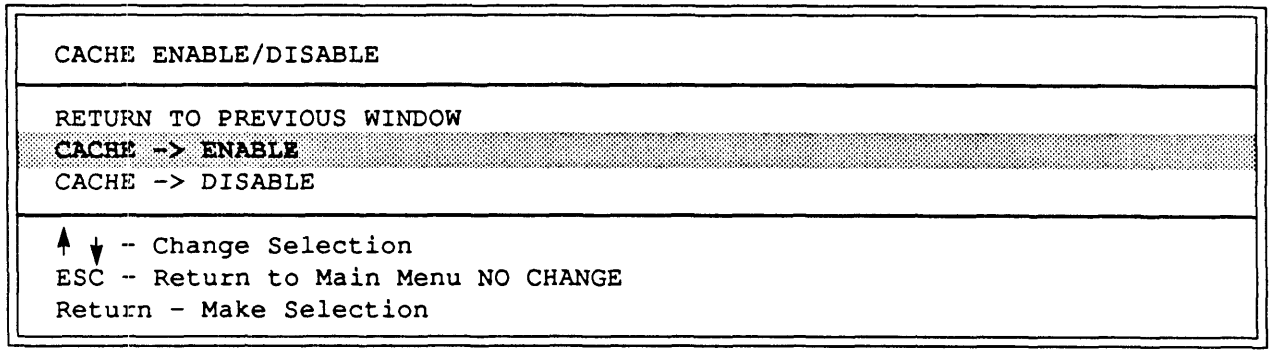
240-36

Figure D-7C. Remap 256K Memory ENABLE/DISABLE



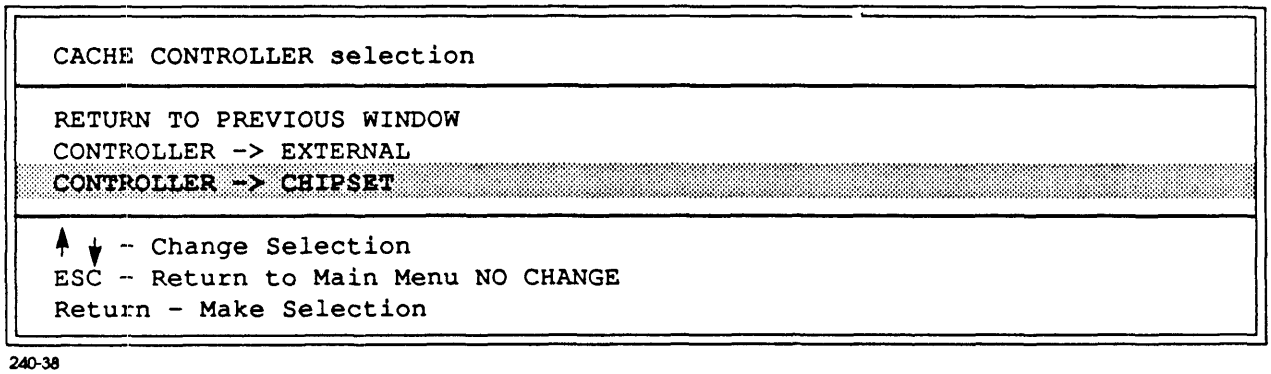
240-30

Figure D-8. OPTI Cache Configuration Setting



240-37

Figure D-8A. Cache ENABLE/DISABLE



240-38

Figure D-8B. Cache Controller Selection

```
256K REMAPPED AREA CACHEABLE ENABLE/DISABLE

RETURN TO PREVIOUS WINDOW
256K CACHEABLE -> ENABLE
256K CACHEABLE -> DISABLE

↑ ↓ - Change Selection
ESC - Return to Main Menu NO CHANGE
Return - Make Selection
```

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Figure D-8C. 256K Remapped Area Cacheable ENABLE/DISABLE

```
RETURN TO PREVIOUS WINDOW
RANGE -> 1M CACHEABLE AREA
RANGE -> 2M CACHEABLE AREA
RANGE -> 3M CACHEABLE AREA
RANGE -> 4M CACHEABLE AREA
RANGE -> 5M CACHEABLE AREA
RANGE -> 6M CACHEABLE AREA
RANGE -> 7M CACHEABLE AREA
RANGE -> 8M CACHEABLE AREA
RANGE -> 9M CACHEABLE AREA
RANGE -> 10M CACHEABLE AREA
RANGE -> 11M CACHEABLE AREA
RANGE -> 12M CACHEABLE AREA
RANGE -> 13M CACHEABLE AREA
RANGE -> 14M CACHEABLE AREA
RANGE -> 15M CACHEABLE AREA
RANGE -> 16M CACHEABLE AREA

↑ ↓ - Change Selection
ESC - Return to Main Menu NO CHANGE
Return - Make Selection
```

NOTE: Set the RANGE to the amount of memory installed in the system.

240-40

Figure D-8D. Cacheable Address Range

Appendix E
80486-25 MOTHERBOARD CONFIGURATION

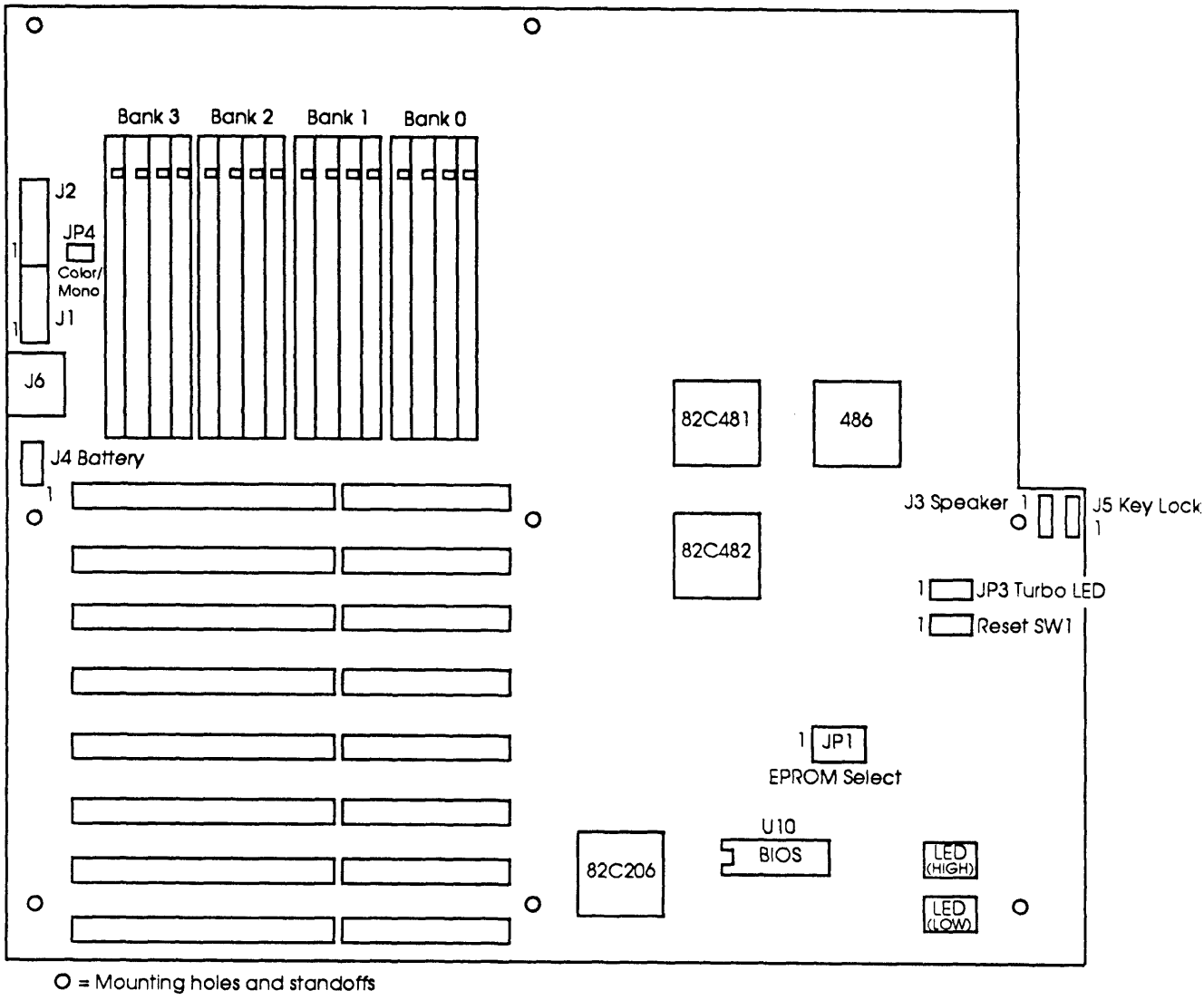


Figure E-1. 80486-25 Motherboard Layout

Table E-1. 80486-25 Jumpers and Switch Settings

J1	6-pin power connector
	Pin 1 – Orange Pin 2 – Red Pin 3 – Yellow Pin 4 – Blue Pin 5 – Black Pin 6 – Black
NOTE: Power connectors should be plugged in with black wires in middle of J1/J2 connector.	
J2	6-pin power connector
	Pin 1 – Black Pin 2 – Black Pin 3 – White Pin 4 – Red Pin 5 – Red Pin 6 – Red
J6	5-pin DIN socket keyboard connector
J4	Battery Connector
	Pin 1 – Battery positive Pin 2 – Key Pin 3 – Ground Pin 4 – Ground
U10	EPROM (BIOS) 512K
JP4	COLOR/MONO selection
	IN Color (eg. VGA/EGA) OUT MONO
JP1	256K/512K EPROM BIOS
	Connect JP1-1 and JP1-2 – 512K EPROM BIOS Connect JP1-2 and JP1-3 – 256K EPROM BIOS
JP3	TURBO LED
	JP3-1 and JP3-3 is VCC connecting to LED Anode. JP3-2 connecting to LED Cathode.
J3	Speaker
	J3-1 Speaker Data J3-2 Key (No connection) J3-3 Ground J3-4 VCC
J5	KEYLOCK LED
	J5-1 VCC J5-2 Key (No connection) J5-3 Ground J5-4 Key Board Lock J5-5 Ground
SW1	RESET SWITCH

```
Cache Computers Inc.  BAT486 BIOS                     Ver V1.04  Port CCI 402
 Summary   Clock    Video   Floppy   Fixed   Boot-Seq  Keyboard   More---

 CPU ....................80486-01     Floppy 0 (A:) ...........1.2M 6mS
 MHz .........................25.0     Floppy 1 (B:) ..............None
 NPX ....................Built-in     Fixed 80 (C:) .............Type 1
 CPU Speed ....................n/a    Fixed 81 (D:) ..............None

 RAM Cache .................Enable    Boot Sequence ............A:  1st
 Shadow RAM ................Enable    Cold-Boot Delay ............0 Sec
 Memory-Base .................640K
 Memory-Extended ...........15360K    Keyboard .......................AT
 Memory-System ...............384K    NumLock ........................On
 Memory-Total ..............16384K    Typematic ................Default

 COM1 .........................n/a    Video-Primary .........Monochrome
 COM2 .........................n/a    Video-Secondary .......CGA - Fast
 LPT1 .........................3BC
 LPT2 .........................n/a    Security .................Disable
 LPT3 .........................n/a

          F10 to Record and Exit             Home End Moves Cursor
```

240-42

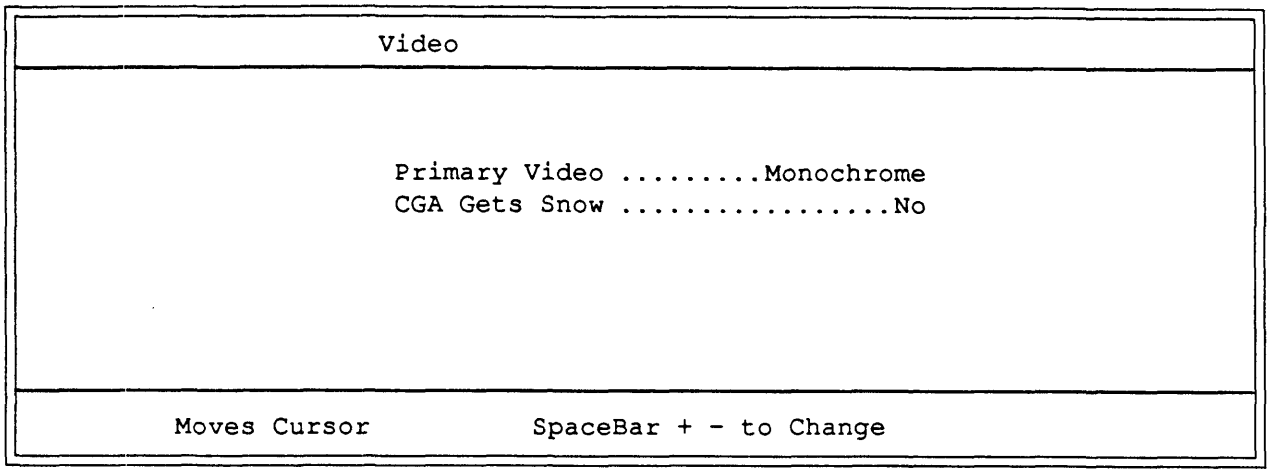
Figure E-2. 80486-25 CMOS Setup Summary

```
Cache Computers Inc.  BAT486 BIOS                     Ver V1.04  Port CCI 402
            Clock

                     Time  hh:mm:ss t ..............11:28:20 a
                     Date  mm/dd/yyyy ...............09/06/1990
                     Daylight Savings ..................Enable

          Moves Cursor         DY to Edit
```

240-44

Figure E-3. 80486-25 CMOS Setup – Clock

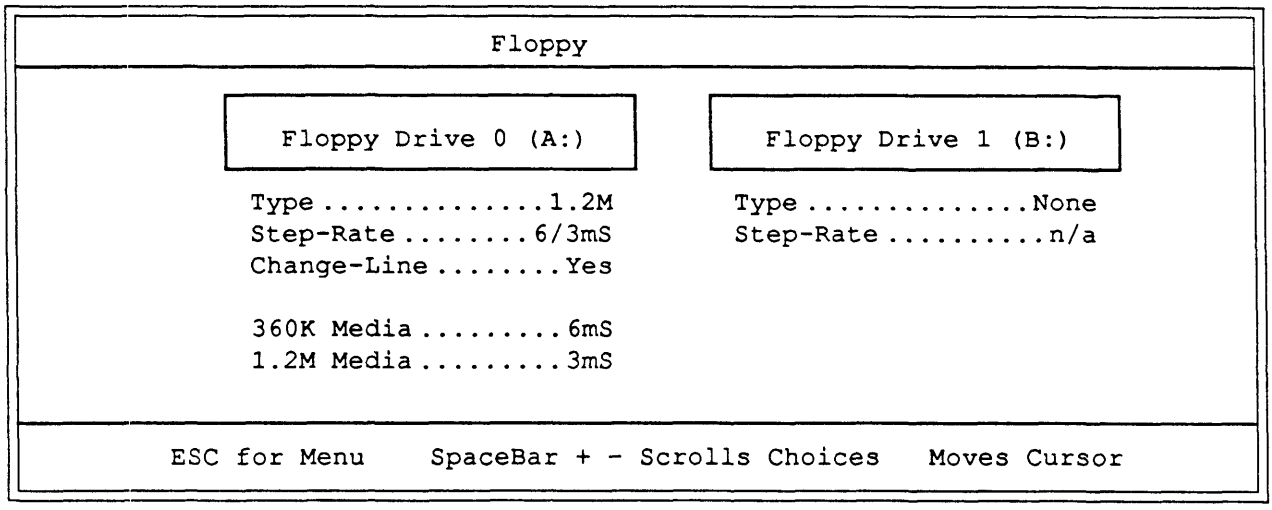
Cache Computers Inc. BAT486 BIOS Ver V1.04 Port CCI 402



240-43

Figure E-4. 80486-25 CMOS Setup - Video

Cache Computers Inc. BAT486 BIOS Ver V1.04 Port CCI 402



240-45

Figure E-5. 80486-25 CMOS Setup - Floppy

```
Cache Computers Inc.  BAT486 BIOS                    Ver V1.04  Port CCI 402

                                  Fixed

  Fixed Disk 80 (C:)          (Low Level) Format        Fixed Disk 81 (D:)

  Type ............1          Drive (C/D) .....*        Type .........None
  Cylinders .....306          Start Cyl .......*        Cylinders .....n/a
  Heads ...........4          Final Cyl .......*        Heads .........n/a
  Precomp .......128          Interleave ......*        Precomp .......n/a
  Landing .......305          Ready (y/n) .....*        Landing .......n/a
  Sectors ........17                                    Sectors .......n/a
  Translate ......No                                    Translate .....n/a
  Step-Rate .......0                                    Step-Rate .....n/a

  0 = No Drive      1-45 = Built-in Table     46,47 = User Programmable

     ESC for Menu   CTRL-F Format   Cursor   + - Scroll Type   DY to Edit
```

240-46

Figure E-6. 80486-25 CMOS Setup – Fixed

```
Cache Computers Inc.  BAT486 BIOS                    Ver V1.04  Port CCI 402

                                  Boot-Seq

        Boot Sequence .....................A:  1st, C:  2nd
        Cold-Boot Delay ..............................None

        Cold-Boot Key Sequence
        DY ..........................Boot to Screen Prompt
        ESC .........................Boot to Setup Utility

        Warm-Boot Key Sequence
        CTRL ALT DEL ................Standard Warm Restart
        CTRL ALT INS ................Instant! WArm Restart
        CTRL ALT DY .................Boot to Screen Prompt
        CTRL ALT ESC ................Boot to Setup Utility

          Moves Cursor          SpaceBar + - to Change
```

240-47

Figure E-7. 80486-25 CMOS Setup – Boot-Sequence

```
Cache Computers Inc.  BAT486 BIOS                    Ver V1.04  Port CCI 402

                                                          Keyboard

                    Powerup Numlock .....................Enable
                    Typematic Override ..................Disable
                    Delay Before Repeat .................Default
                    Typematic Repeat Rate ...............Default

          Moves Cursor          SpaceBar + - to Change
```

240-48

Figure E-8. 80486-25 CMOS Setup – Keyboard

```
Cache Computers Inc.  BAT486 BIOS                    Ver V1.04  Port CCI 402

                          First-Aid

                    Novell Keyboard Problem ..................No

  Select the lowest numeric value allowing the keyboard to operate properly.

          ESC for Menu          SpaceBar + - Scrolls Choices
```

240-49

Figure E-9. First-Aid

```
Cache Computers Inc.  BAT486 BIOS                       Ver V1.04  Port CCI 402

                         Cache

              Internal Cache .......................Enable
              External Cache .......................Enable

                   Runtime Hot-Key Sequence

              CTRL ALT SHIFT - ..............Disable Cache
              CTRL ALT SHIFT + ...............Enable Cache

        Moves Cursor          SpaceBar + - to Change
```

240-50

Figure E-10. Cache

```
Cache Computers Inc.  BAT486 BIOS                       Ver V1.04  Port CCI 402

                                  Shadow

                  F000 BIOS ...................WP-Shadow

                  E000 SYSTEM ....................Vacant

                  DC00 ADAPTOR ...................Vacant
                  D800 ADAPTOR ...................Vacant
                  D400 ADAPTOR ...................Vacant
                  D000 ADAPTOR ...................Vacant

                  CC00 ADAPTOR ...................Vacant
                  C800 ADAPTOR ...................ROM #1
                  C400 VIDEO .....................Vacant
                  C000 VIDEO .....................Vacant

   WP = Write-Protect                                      RW = Read/Write

        Moves Cursor          SpaceBar + - to Change
```

240-51

Figure E-11. Shadow

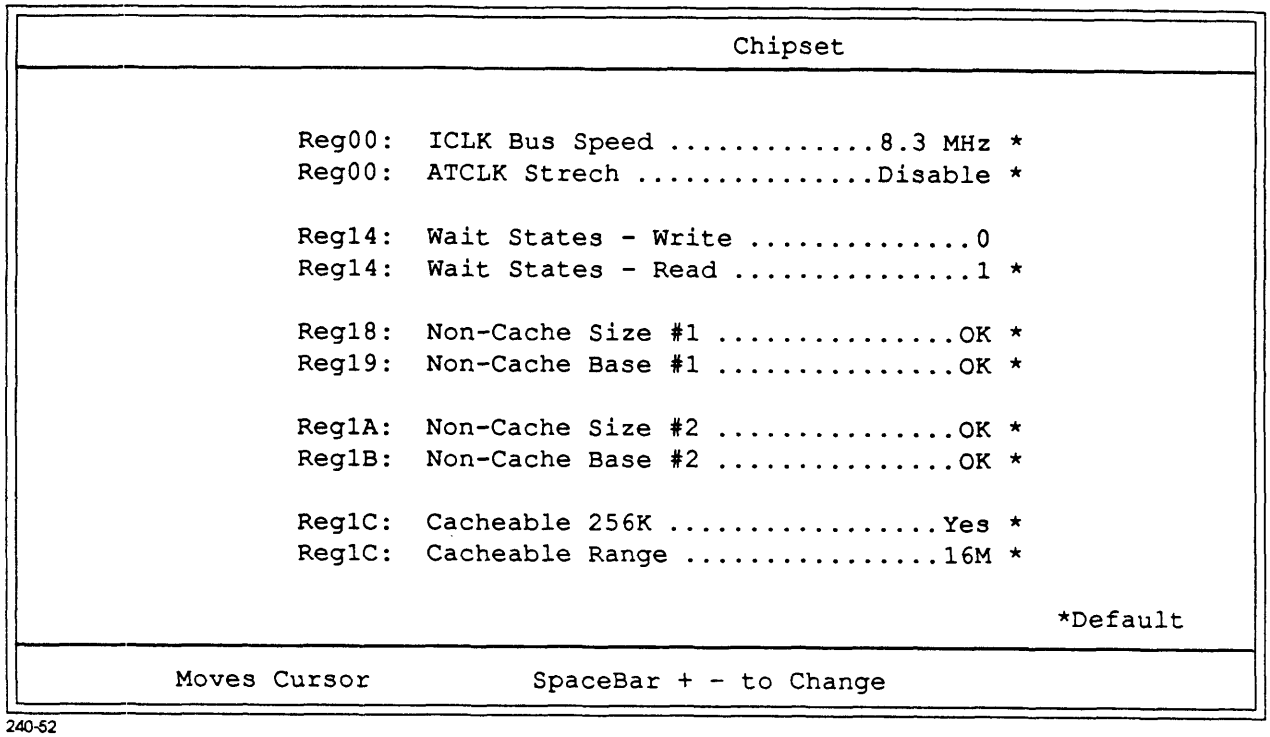


Figure E-12. Chipset

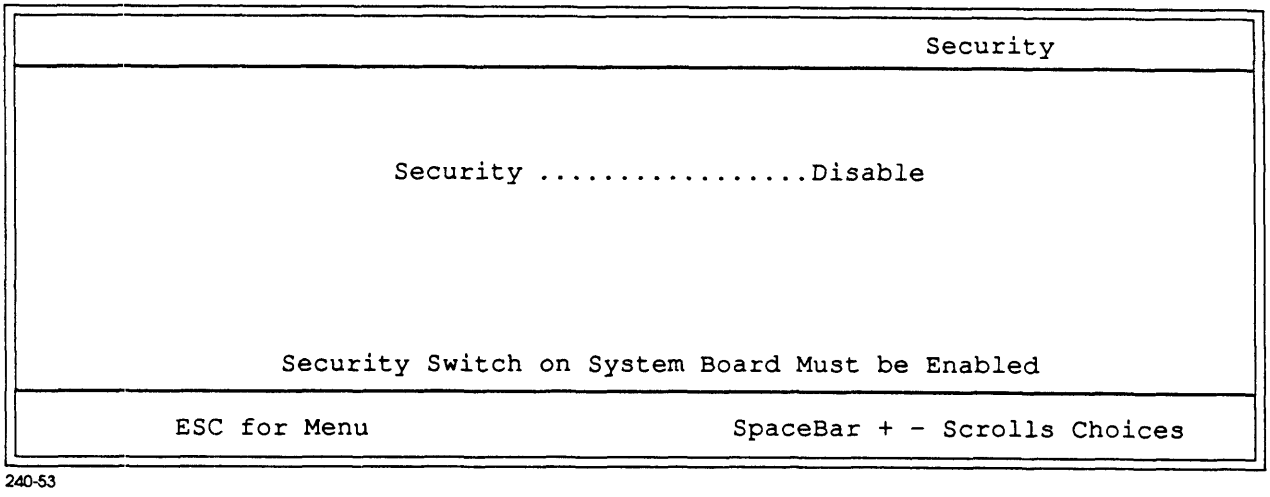


Figure E-13. Security

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