REVISION HISTORY		
ECO #	DATE	DESCRIPTION
0115	4/25/83	Changed Page 11
0328	6/28/84	New ZETACO Cover

CUSTOMER SERVICE

Our warranty attests the quality of materials and workmanship in our products. If malfunction does occur, our service personnel will assist in any way possible. If the difficulty can not be eliminated by use of the following service instructions and technical advise is required, please phone the Custom Systems sales department (612-941-9480) giving the serial number, board name, model number, and problem description. You will be placed in contact with the appropriate technical assistance.

PRODUCT RETURN

Pre-return Checkout.

If controller malfunction is suspected, the use of test software is needed to determine if the controller is the problem and what in particular is wrong with the controller. The tests applicable to this board are listed on the next page of the manual. Please run the test sequence before considering product return.

Returned Material Authorization.

Before returning a product to Custom Systems for repair, please ask our sales secretary for a "Returned Material Authorization" number. Each product returned requires a separate RMA number. Use of this number in correspondence and on a tag attached to the product will ensure proper handling and avoid unnecessary delays.

Returned Material Information.

Information concerning the problem description, system configuration, diagnostic program name, revision level, and results, i.e., error program counter number should be included with the returning material. A form is provided for this information on the next page of the manual.

Packaging.

To safeguard your materials during shipment, please use packaging that is adequate to protect it from damage. Mark the box "Delicate Instrument" and indicate the RMA number(s) on the shipping label.

(Include with returning material)

MATERIAL RETURN INFORMATION

All possible effort to test a suspected malfunctioning controller should be made before returning the controller to Custom Systems, Inc. for repair. This will: 1) Determine if in fact the board is defective (many boards returned for repair are not defective, causing the user unnecessary system down-time, paper work, and handling while proper testing would indicate the board is working properly). 2) Increase the speed and accuracy of a product's repair which is often dependent upon a complete understanding of the user checkout test results, problem characteristics, and the user system configuration. Checkout results for the QTY Multiplexer should be obtained by performing the following tests. (Include error program counter #'s and accumulator contents if applicable).

TEST	RESULTS
QTYDR	

Other tests performed:

Please allow our service department to do the best job possible by answering the following questions thoroughly and returning this sheet with the malfunctioning board.

1. Does the problem appear to be intermittent or heat sensitive? (If yes, explain).

   _____

2. What operating system are you running under? (AOS RDOS, DDOS, DTOS).

   _____

3. Describe the system configuration (i.e., peripherals, I/O controllers, model of computer, etc.

   _____

   _____

4. Has the controller been returned before? _____ Same problem?_____

   To be filled out by CUSTOMER:

   Model #: _____

   Serial #: _____

   RMA #: _____

   Returned by:_____
   (company name)

TABLE OF CONTENTS

Section 1 Introduction

The Custom Systems Series 260 Asynchronous Multiplexor Controller enables any Data General Nova or Eclipse line computer to communicate with and control up to eight (8) serial terminal devices (i.e., CRT, teletypes) and four (4) data sets (modems). The multiplexor controller contains all the circuitry necessary to receive, transmit and buffer the data characters between the terminal devices and the computer. From one to eight cards serving up to 64 lines operate together as a multiplexing system. The multiplexor controller is contained on a 15 x 15 card and installs directly into the Nova or Eclipse logic chassis, thus eliminating the need for auxiliary power supplies and cabinet. The multiplexor is compatible with Data General's operating system and diagnostic software.

Section 2 Configurations

The multiplexor controller is configured into the following models and cable assemblies:

Model No.	Description
260-4	Four (4) channel multiplexor with individual baud rate, data format selection and RS-232 or current loop interface. Baud rate selection using dip switches is available as an option.
260-8	Eight (8) channel multiplexor with individual baud rate, data format selection and RS-232 or current loop interface. Baud rate selection using dip switches is available as an option.
260-M	Full modem control circuitry for four (4) lines. This configuration is added to the 260-4 or 260-8.
260-C-4	Internal cable and panel assembly for 260-4.
260-C-8	Internal cable and panel assembly for 260-8.

Section 3 Theory of Operations

Section 3.1 General

In communicating with the serial terminal devices, the multiplexor hardware performs all character assembly and disassembly into the serial bit streams

required. Start and stop bits are inserted on transmission and stripped out on reception. Character buffering is provided on both reception and transmission so that the program has a full character time to respond without losing input data or reducing transmission rate.

The multiplexor system is flexible in line capacity, transmission code and line speed. It can accommodate from four to 64 full duplex lines, in multiples of four or eight at speeds up to 19,200 baud. The transmission code structure (character size and number of stop bits) and line speeds are selectable by the user so that an installation can be reconfigured with minimal hardware change.

A number of four-line or eight-line multiplexor cards appear as if they were a single I/O device connected to the computer under a single device code. On reception, an I/O instruction reads words containing the line number in the left half and a character in the right. At the completion of transmission of a character, an I/O instruction reads a similar word containing the line number indicating that a character has been transmitted. The program responds by outputting a word containing the appropriate line number and new character. Multiplexing occurs since the I/O instruction to read a line number/character word and control information always affects only one line on one of several cards. The choice of which of several cards is made automatically by the hardware in priority order, lower line numbers having the higher priority.

Section 3.2 Circuit Descriptions

Section 3.2.1 Clock Oscillator and Baud Rate Divider Chain

The clock oscillator is a crystal-controlled series resonant oscillator and operates at 3.072 MHZ. Chip N12 divides the clock oscillator frequency by 10 and then feeds the baud rate divider chain and the I/O reset logic.

The baud rate divider chain (Chips L7, M7 and N7) further divides the clock oscillator into the frequencies required for the various baud rates. Note that the clock frequency is 16 times the baud rate. Divider chain outputs are

connected to the baud rate jumpers or optional switches to accommodate jumpering the required baud rates for each line. Baud rate jumper locations and line numbers are listed.

Jumper Location	Line No.
A7	0
B7	1
C7	2
D7	3
G7	4
H7	5
J7	6
K7	7

The I/O reset logic is a pulse-forming network on the computer interface I/O term IORST.

Section 3.2.2 Computer I/O Interface

The interface provides decoding of the I/O instructions, multiplexor selection, line selection and data interface.

Multiplexor selection (MUX SEL) and line selection (SEL GROUP) are gated with the necessary I/O instructions to insure the correct communications link is established.

Mask Bit 14 is used to mask interrupts from the multiplexor.

The multiplexor selection logic decodes the DS0-DS5 lines for either a 30_8 or 70_8 device code. When selection is made, Chip B1-Pin 8 goes low and stays low as long as the proper decode is maintained.

The line selection logic exclusive ores data lines bits 2 through 5 and the hard wired line addresses on the board. When the data lines match the hard wired address, Chip G1-Pin 4 goes low and term GRP becomes true. This indicates a particular group of four or eight lines has been selected. GRP is added with MUX SEL at Chip F4; and, when Pin 1 becomes active (SEL GROUP), it indicates that the MUX and a group of lines (4 or 8) are selected.

The data interface is an open collector interface connected to the computer's common data bus. The multiplexor uses the data interface for received data, transmitted data, line number and the transmit/receive indicator.

Section 3.2.3 Data Transfer

This section encompasses the character assembly and disassembly logic, the busy/done logic and the line priority logic.

The heart of the character assembly and disassembly logic is the universal asynchronous receiver/transmitter chip (UART). The UART can be separated into a transmitter section and a receiver section and is capable of full duplex (simultaneous transmission and reception) or half duplex operation.

All lines operate similarly and, therefore, line 0 will be used as a representative line in the descriptions.

(Reference transmitter timing diagram for following description.)

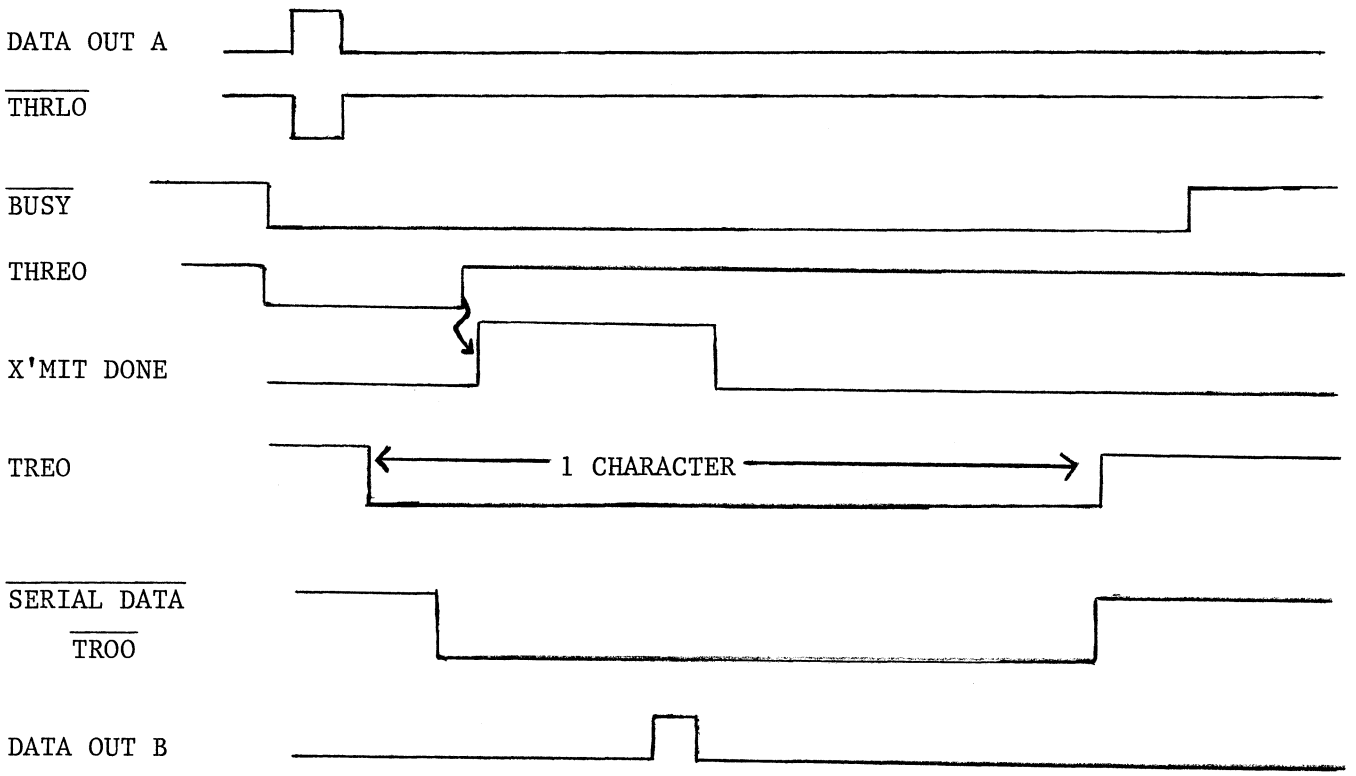
The transmitter section basically disassembles parallel data from the computer into serial asynchronous data for the terminal device.

The data lines, bits 8 through 15, are connected to all the UARTs. Data is loaded into the UARTs by the Data Out A command. Loading the correct UART is accomplished by a 1 of 8 decoder (Chip D6) which provides a THRL pulse only for the addressed line. In our example, THRL0 would become active and load UART "0" buffer register (Chip A10).

THRLO also sets the Busy F/F (ChipA8) indicating a data transfer is in progress. Data is then transferred from the UART's buffer register to its transmitter register. At this time, THREO becomes active and sets the X'mit Done F/F (Chip C8). Data begins to serially shift out of the transmitter register (TRO) and is outputted at current loop or RS-232 logic levels. The Start, Parity and Stop bits are automatically appended to the serial data by the UART's control circuitry which is jumper controlled. UART control pins 35 through 39 are jumperable so that the characters may be 5, 6, 7 or 8 bits in length, have 1, 1½ or 2 stop bits and have odd, even or no parity bit.

As previously mentioned, THREO sets the X'mit Done F/F. This F/F can be cleared by IORESET or DOBO, DOBO being Data Out B gated by the selected line (Chip H6).

At the completion of the transmission of a data character, TREO becomes active and clears the Busy F/F. This completes the transmission cycle.



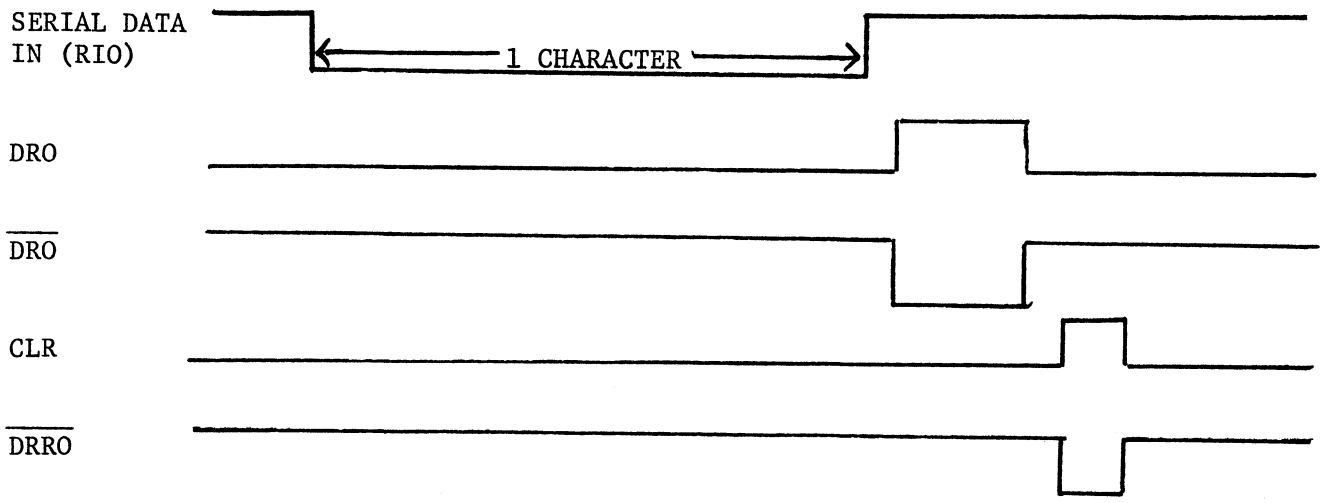
TRANSMITTER TIMING

(Reference the receiver timing diagram for the following description.)

The receiver section assembles the asynchronous data characters into a parallel character and outputs the character to data bits 8 through 15 with the Start, Parity and Stop bits removed.

Serial data (RIO) enters the UART buffer register from the line receiver. When an entire character has been assembled, DRO goes high indicating that the character has been transferred to the UART's holding register. DRO is equivalent to a Receive Done F/F. The Receive Done (DRO) is processed through the priority chain and DRO enables the parallel output of UART "0" holding register. (All the UART's holding registers are wired together, and enabling the DRX input enables that particular UART to output its holding register on the Data Bus Bit 8 through 15.)

A Clear pulse (Chip M9) DRRO disconnects UART's "0" holding register from the data bus and resets DRO (the Receive Done F/F).



RECEIVER TIMING

The card Busy is an "OR" gate of the 8 individual lines Transmit Busy. Any line being Busy produces a card Busy (Chip N8).

The card Done may be either a Transmit Done (TDO) or a Receive Done (DRO). Any line with Transmit Done or Receive Done active produces a card Done (Chip F5-Pin 15).

The priority logic is priority on the Transmit or Receive Dones. It assigns the highest priority to the lower number lines (i.e., Line 0 has higher priority than line 2). Transmit Done (TDO) or Receive Done (DRO) is continuously strobed by REQB in the priority network. If a higher priority Done does not exist, a lower order $\overline{\text{DRX}}$ is allowed. As previously mentioned, the 8 lines of $\overline{\text{DRX}}$ connect to Chip F5 to provide a card Done. Chip F5 also encodes the $\overline{\text{DRX}}$ into a binary representation. This binary representation (IN0, IN1, IN2) provides selection logic to Chips A3 and M6 to select the transmit/receive indicator and line address information during a Data In A instruction.

Section 3.2.4 Terminal Device Interface

The terminal device output can be either 20 MA current loop or RS-232C output. A jumper option is available for ease of conversion. If this option is required, inform Custom Systems at the time of ordering. If Custom Systems is not informed that this conversion is a customer requirement, the boards will be shipped as RS-232C output only.

Section 4 Installation and Options

Section 4.1 Installation

Inspect the multiplexor board for any damage which may have occurred in transit. Immediately notify the involved carrier if damage is observed.

Recheck option requirements to ensure the options originally specified are still correct. Install and recheck cabling to the board to ensure correct

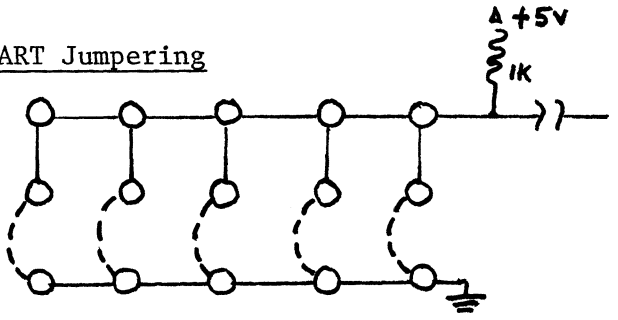
connections. Install multiplexor board in the Nova or Eclipse logic chassis.

NOTE: When using Custom Systems internal cable and panel assembly 260-C-4 or 260-C-8, the following interface circuits cabling should be noted:

Internal Cable	Description	Connect to External Cable (Customer Supplied)
Connecting CRT's to the cable and panel assembly:		
Pin 2	Transmitted data	Pin 3
Pin 3	Received data	Pin 2
Connecting modems to the cable and panel assembly:		
Pin 2	Transmitted data	Pin 2
Pin 3	Received data	Pin 3

Section 4.2 Jumper Options (Reference Jumper Option Sheet in Schematics)

Section 4.2.1 UART Jumpering



____ = Primary Jumper

---- = Alternate Jumper

To install alternate jumper, cut primary jumper (foil) and install insulated wire as shown.

Listed below are the jumper options associated with each UART.

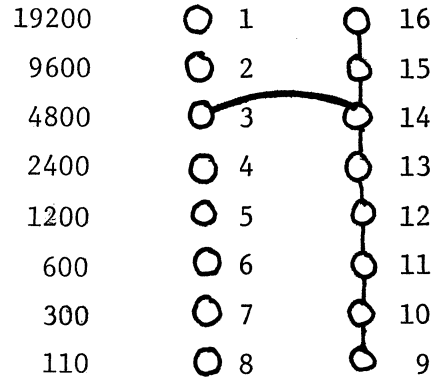
UART PIN #	PRIMARY (Hi)	ALTERNATE (Lo)
35	Inhibits parity generation and verification	Allows parity generation and verification
36	Two stop bits *When 5-bit word is programmed, 1.5 stop bits are generated.	One stop bit

UART PIN #37	UART PIN #38	WORD LENGTH
Alternate (Lo)	Alternate (Lo)	5 Bits
Alternate (Lo)	Primary (Hi)	6 Bits
Primary (Hi)	Alternate (Lo)	7 Bits
Primary (Hi)	Primary (Hi)	8 Bits

UART PIN #	PRIMARY (Hi)	ALTERNATE (Lo)
39	Even Parity	Odd Parity

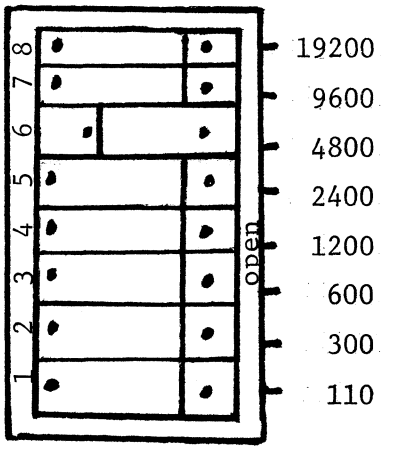
Unless specified, primary jumpers are installed at the time of shipment.

Section 4.2.2 Baud Rate Jumpering (Reference Jumper Option Sheet in Schematics)



4800 Baud Shown
Pin 3 to Pin 14

Optional Switch



4800 Baud Shown
Switch 6 Closed

For each line, 8 baud rates are selectable. Listed are the pins to jumper for each baud rate.

Baud Rate	Jumper Pins	Switch Closed
19200	1 to 16	8
9600	2 to 15	7
4800	3 to 14	6
2400	4 to 13	5
1200	5 to 12	4
600	6 to 11	3
300	7 to 10	2
110	8 to 9	1

Unless specified, 4800 baud is selected at the time of shipment.

Section 4.2.3 Multiplexor Address Jumpering (Reference Jumper Option Sheet in Schematics)

Two addresses are available - 30_8 and 70_8

30_8 = No jumper

70_8 = Insulated jumper installed

Unless specified, address 30_8 is selected at the time of shipment.

Section 4.2.4 4 Channel/8 Channel Jumpering (Reference Jumper Option Sheet in Schematics)

Two jumpers - One by Chip N2 (J101); the other by Chip G1 (J340)

NOTE: The jumper by Chip N2 is shown in Section 4.2.6. When instructions specify a jumper, install at the dashed line (---).

4 Channel Board = No J101 Jumper - No J340 Jumper (Chip G1)

8 Channel Board = J101 Jumper - No J340 Jumper (Chip G1)

8 Channel Board = No J101 Jumper - J340 Jumper (Chip G1)
(Using only 4 Channel)

4 Channel or 8 Channel must be specified at the time of order.

Section 4.2.5 RS-232/Current Loop Jumpering (Reference Jumper Option Sheet in Schematics)

Each line may have either RS-232C or current loop output. The capability to field change between RS-232C and current loop must be specified at the time of order. If not specified at the time of order, the conversion must be done at the factory.

If the board is ordered as field convertible, use below instructions.

RS-232C to Current Loop (Reference Schematics)

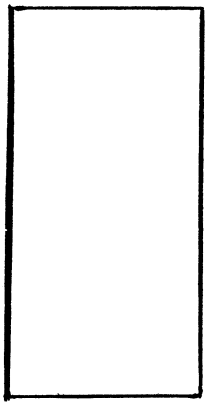
	Install Jumpers	Remove Jumper
Line 0	J200 and J280	J201
Line 1	J220 and J281	J221
Line 2	J240 and J282	J241
Line 3	J260 and J283	J261
Line 4	J300 and J381	J301
Line 5	J320 and J382	J321
Line 6	J342 and J383	J341
Line 7	J361 and J384	J362

Current Loop to RS-232C (Reference Schematics)

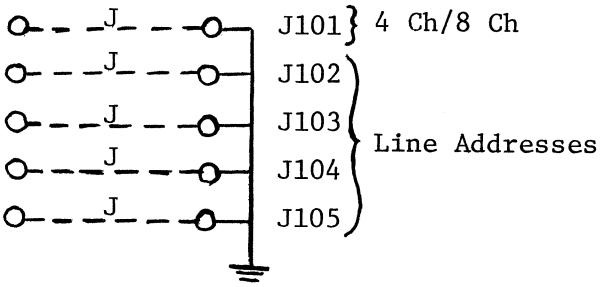
	Install Jumper	Remove Jumpers
Line 0	J201	J200 and J280
Line 1	J221	J220 and J281
Line 2	J241	J240 and J282
Line 3	J261	J260 and J283
Line 4	J301	J300 and J381
Line 5	J321	J320 and J382
Line 6	J341	J342 and J383
Line 7	J362	J361 and J384

Section 4.2.6 Line Address Jumpering (Reference Jumper Option Sheet in Schematics)

Up to 64 addresses are available (4/8 addresses per multiplexor board).



Chip N2



4 Channel Multiplexor

	J105 (2^2)	J104 (2^3)	J103 (2^4)	J102 (2^5)
Line 0 - 3	--	--	--	--
4 - 7	J	--	--	--
8 - 11	--	J	--	--
12 - 15	J	J	--	--
16 - 19	--	--	J	--
20 - 23	J	--	J	--
24 - 27	--	J	J	--
28 - 31	J	J	J	--
32 - 35	--	--	--	J
36 - 39	J	--	--	J
40 - 43	--	J	--	J
44 - 47	J	J	--	J
48 - 51	--	--	J	J
52 - 55	J	--	J	J
56 - 59	--	J	J	J
60 - 63	J	J	J	J

8 Channel Multiplexor

	J105 (2^2)	J104 (2^3)	J103 (2^4)	J102 (2^5)
Line 0 - 7	--	--	--	--
8 - 15	--	J	--	--
16 - 23	--	--	J	--
24 - 31	--	J	J	--
32 - 39	--	--	--	J
40 - 47	--	J	--	J
48 - 55	--	--	J	J
56 - 63	--	J	J	J

-- = No Jumper

J = Insulated Jumper

Unless specified, lines 0 - 3/7 are selected at time of shipment.

Section 4.2.7 Priority Jumper When There Are Multiple Multiplexor Boards Per Computer

This backpanel jumper allows priority assignment. Jumper Pin A-91 of higher priority board to A-92 of a lower priority board.

Section 5 Interface

Section 5.1 Computer/Interface

Signal	Card Slot Pin
CLR	A50
DATA 0	B62
DATA 1	B65
DATA 2	B82
DATA 3	B73
DATA 4	B61
DATA 5	B57
DATA 6	B95
DATA 7	B55
DATA 8	B60
DATA 9	B63
DATA 10	B75
DATA 11	B58
DATA 12	B59
DATA 13	B64
DATA 14	B56
DATA 15	B66
DATOA	A58
DATOB	A56
DATIA	A44
DCHP IN *	A94
DCHP OUT *	A93
DS0	A72
DS1	A68
DS2	A66
DS3	A46
DS4	A62
DS5	A64
INTA	A40
INTP IN	A96
INTP OUT	A95
INTR	B29
IORST	A70
MSKO	A38
PRI IN	A92
PRI OUT	A91
RQENB	B41
SELB	A82
SELD	A80

* Not used by the multiplexor but is jumpered on the board to maintain data channel priority bus continuity.

Section 5.2 Terminal Device Interface (8 Channel MUX Only)

CLEAR TO SEND CH 0	A75
CH 0 SERIAL DATA IN	A87
CH 0 SERIAL DATA OUT	A85
CLEAR TO SEND CH 1	A77
CH 1 SERIAL DATA IN	A88
CH 1 SERIAL DATA OUT	A86
CLEAR TO SEND CH 2	A76
CH 2 SERIAL DATA IN	A89
CH 2 SERIAL DATA OUT	A83
CLEAR TO SEND CH 3	A78
CH 3 SERIAL DATA IN	A90
CH 3 SERIAL DATA OUT	A84
CLEAR TO SEND CH 4	A79
CH 4 SERIAL DATA IN	A65
CH 4 SERIAL DATA OUT	A67
CLEAR TO SEND CH 5	A81
CH 5 SERIAL DATA IN	A63
CH 5 SERIAL DATA OUT	A69
CLEAR TO SEND CH 6	A57
CH 6 SERIAL DATA IN	A61
CH 6 SERIAL DATA OUT	A71
CLEAR TO SEND CH 7	A49
CH 7 SERIAL DATA IN	A59
CH 7 SERIAL DATA OUT	A73

Section 6 Programming Notes

A receiver indicator (RI) and a transmit indicator (TI) are associated with each line. The receiver indicator is set when a character has been assembled from the serial input stream. It is cleared under program control. The transmit indicator is set whenever the line unit circuitry has accepted a character for transmission and is ready to accept another. I/O reset clears all transmit and receive indicators. Since the transmitter circuitry includes double buffering, the transmit indicator is set almost immediately after accepting the first character following a long idle period. At maximum transmission rate, the transmit indicator is set once per character time; it is cleared under program control.

The eight-line receiver/transmitter cards contain conventional Done flags for interface to a Nova-Line I/O bus. These are logically ored together to get a system Done. To the programmer, Done appears set if any input lines have completely assembled characters ready for reading by the processor (some RI=1) or if any output lines have transmitted characters and can accept new characters (some TI=1).

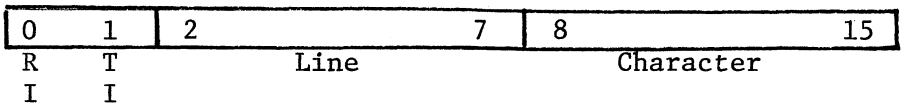
The DIAC instruction, which reads input characters and line control information, also clears the receiver indicator of the line just read. Upon issuance of DIAC AC QTY, Done will be cleared if there are no other lines with data to be read and if all transmit indicators (for all lines) are 0. If there are additional lines to be read or character completions which need to be handled, Done will remain set.

The DOA AC QTY instruction, which supplies a character for output on a selected line, also clears the transmit indicator for that line. If no new character is to be outputted, the DOB AC QTY instruction may be used to clear the transmit indicator without sending a new character. While DOA or DOB clears the transmit indicator for a line, they will clear Done only if there are no other lines on which transmission has completed and if no receivers have assembled characters for the processor to read. The S-pulse is not microcoded as a part of an instruction.

The Busy flag is set whenever output is occurring on any of the lines. It clears when all characters on all lines awaiting transmission have been sent.

I/O Instructions

DIAC AC QTY reads the following word:



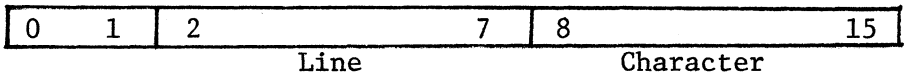
RI = Receive indicator--a character has been assembled and appears in bits 8-15, right justified.

TI = Transmit indicator--a character previously sent to the transmitter has been accepted for transmission and a new character may be sent.

Line = The line number to which the indicators apply.

Character = The character just received on the indicated line if RI is set; undefined if RI is not set.

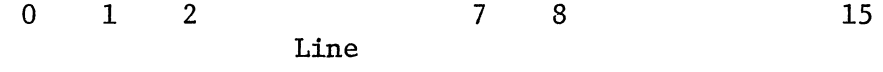
DOA AC QTY assumes the following word in an accumulator:



Line = The line number on which the character is to be transmitted and for which the transmit indicator is to be cleared. Bits 0 and 1 are ignored.

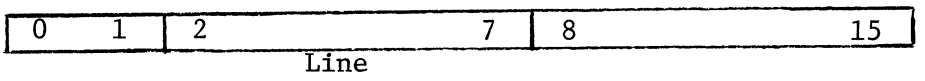
Character = The character to be transmitted; right justified in the byte if less than 8 bits.

DOB AC QTY assumes the following word in an accumulator:



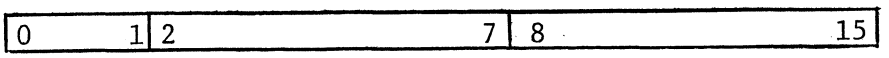
Line = The line number (0 through 7 for a single card system) for which the transmit indicator is to be cleared. Bits 0, 1 and 8 through 15 are ignored.

DOB AC QTY assumes the following word in an accumulator:



Line = The line number (0 through 7 for a single card system) for which the transmit indicator is to be cleared. Bits 0, 1 and 8 through 15 are ignored.

DOB AC QTY assumes the following word in an accumulator:



Line = The line number (0 through 7 for a single card system) for which the transmit indicator is to be cleared. Bits 0, 1 and 8 through 15 are ignored.

Modem Control

The software must monitor the ring indicator (indicates that a ringing signal is being received from the data communications equipment) and Data Set Ready (indicates status of the data communications equipment).

The software controls the state of Data Terminal Ready signal to the data communications equipment. This signal prepares the data communications equipment to be connected to the communication channel and maintains the connection established by external means.

Request To Send to the data communications equipment is active whenever the Done F/F is set or the Busy F/F is set.

DIA AC MDM Senses the state of the Ring Indicator signal from 4 lines. AC Bit 0 On indicates that line 0 is ringing; AC Bit 4 On indicates that line 4 is ringing.

DIB AC MDM Senses the state of the Data Set Ready signal from 4 lines. An AC Bit On indicates that the Data Set is ready; i.e., Bit 0 On indicates Data Set 0 is ready.

DOA AC MDM Controls the state of the Data Terminal Ready signal to each of 4 lines. A logical one in Bits 0 → 3 makes the corresponding line ready.

Model 260

8 Channel Mux

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