

REVISION HISTORY

ECO	DATE	DISCRPTION
0096	2-22-83	SHEETS: 5, 15, 17, 25 AFFECTED
0103	3-10-83	CORRECT SCHEMATICS
0148	6-6-83	SHEETS 2 & 8
0149	6-16-83	SHEETS 4 & 9
0217	1-9-84	SHEET 17 & 20
0258	3-13-84	SHEET 8, 15, 17, 19, 20, 25
0283	3-30-84	SHEET 4
0336	6-29-84	SHEETS 4, 5, 8, 14, 16, 17, 22, 25,
0376	9-6-84	SHEET 17 & 18
0418	12-7-84	SHEETS 4 & 5
0511	10-85	SHEET 25

DC-295C

NOTE :

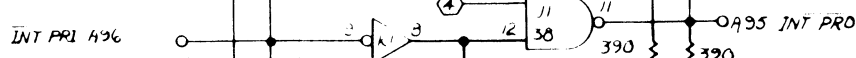
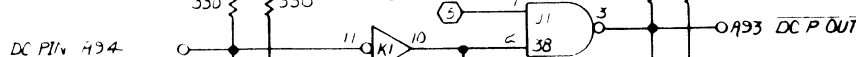
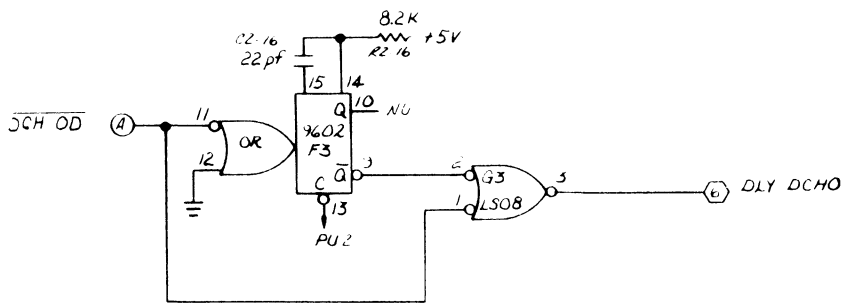
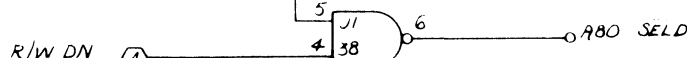
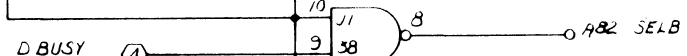
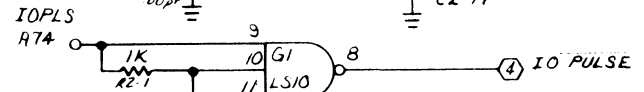
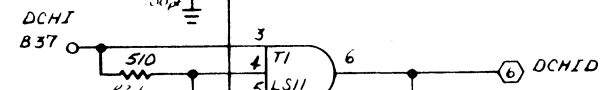
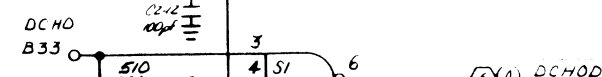
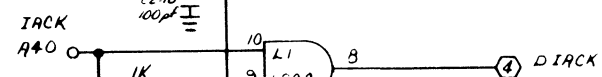
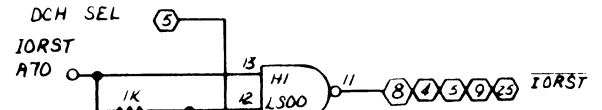
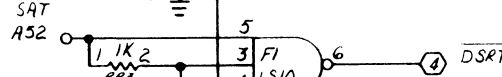
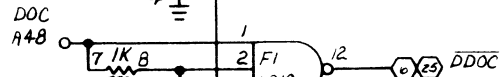
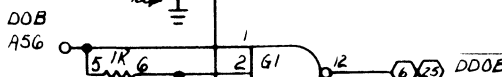
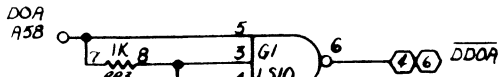
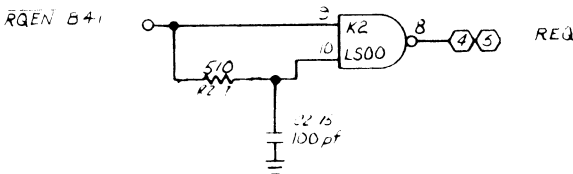
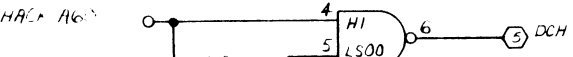
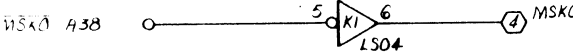
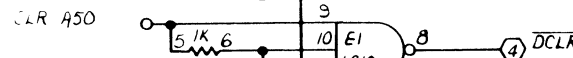
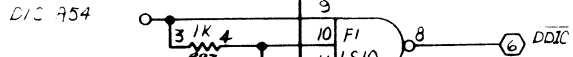
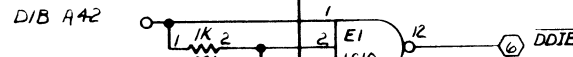
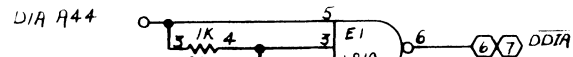
1. NUMBERS FOUND WITHIN THE HEXAGON SYMBOLS INDICATES SHEETS WHERE CONTINUED LOGIC WILL BE FOUND  
 EXAMPLE (2) = SHEET 2

(SHEET 1 OF 25)

<p>700383-0008 ZETACD</p>			
DATE	6-27-85	DESIGNED BY	
APPROVED BY		CHECKED BY	
TITLE	DC-295C	PROCESSING NUMBER	700-383-0008 C

700383-0008

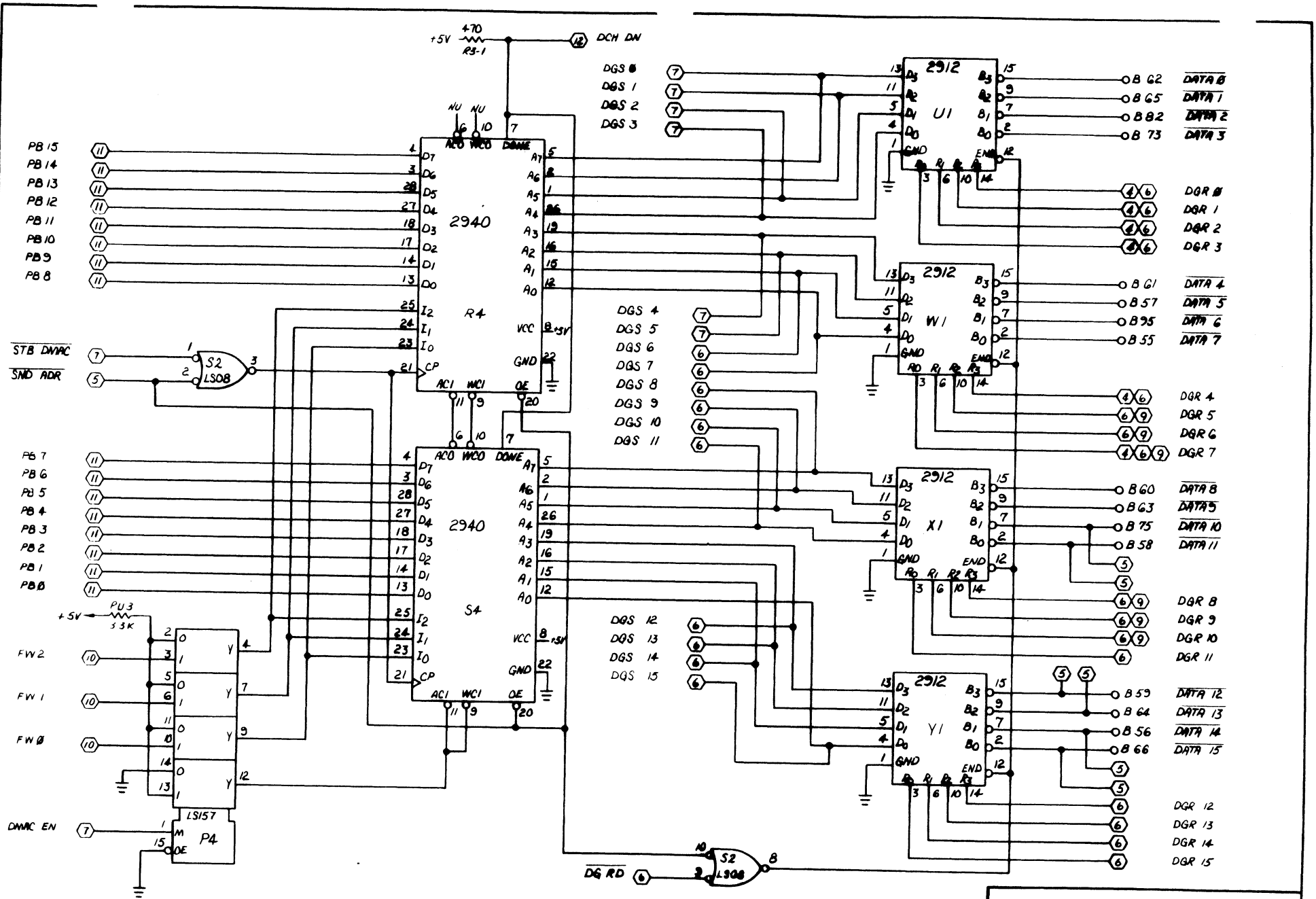
40-2179



(SHEET 2)

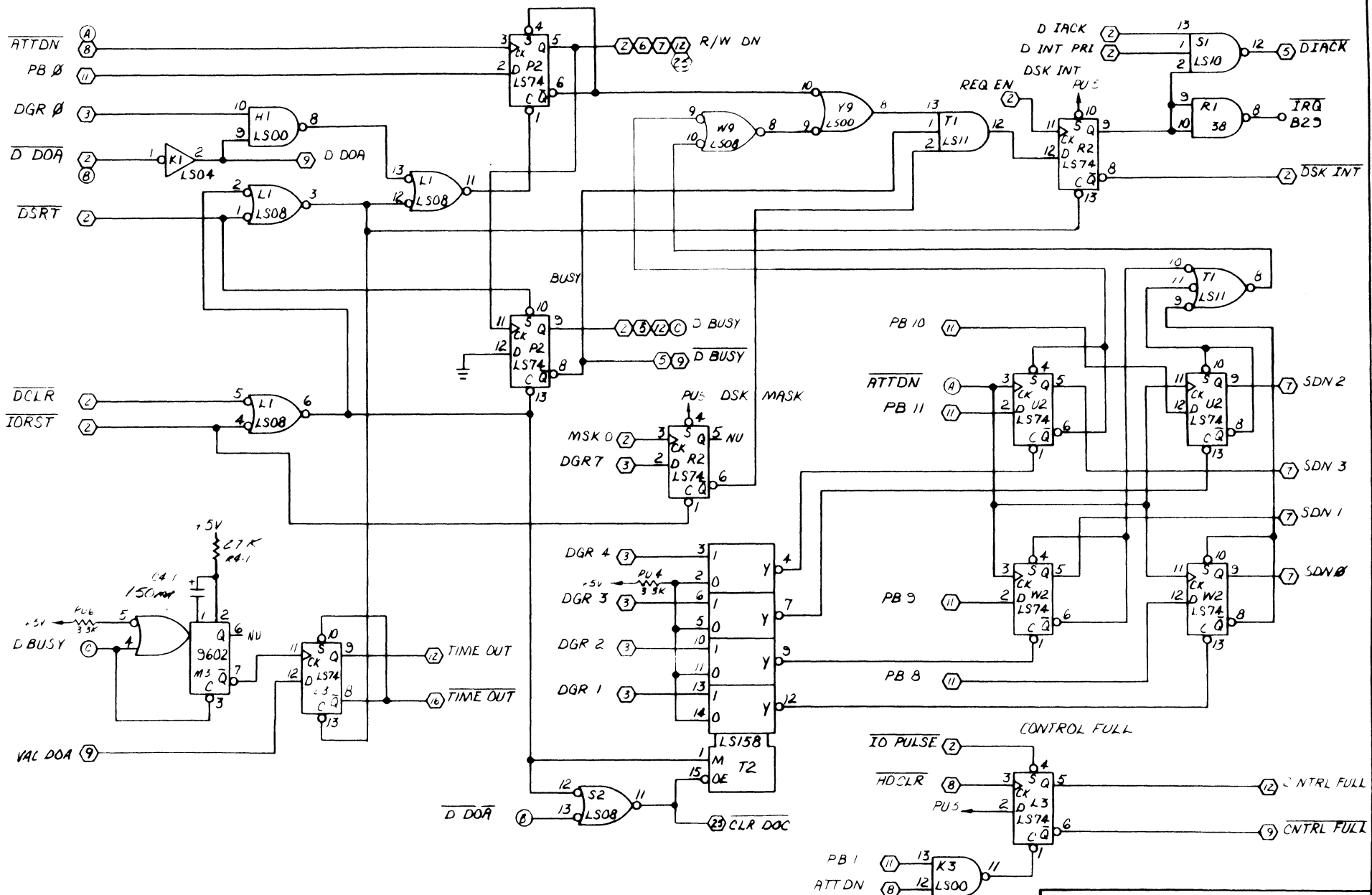
1985 ZETACO

DESIGNED BY C. R. MULL	DATE 3 29 82	REVISIONS	DATE
CHECKED BY			
APPROVED BY			
SCALE			
TITLE DG INTERFACE		DRAWING NUMBER 700-383-00	



**21905 ZETACO**

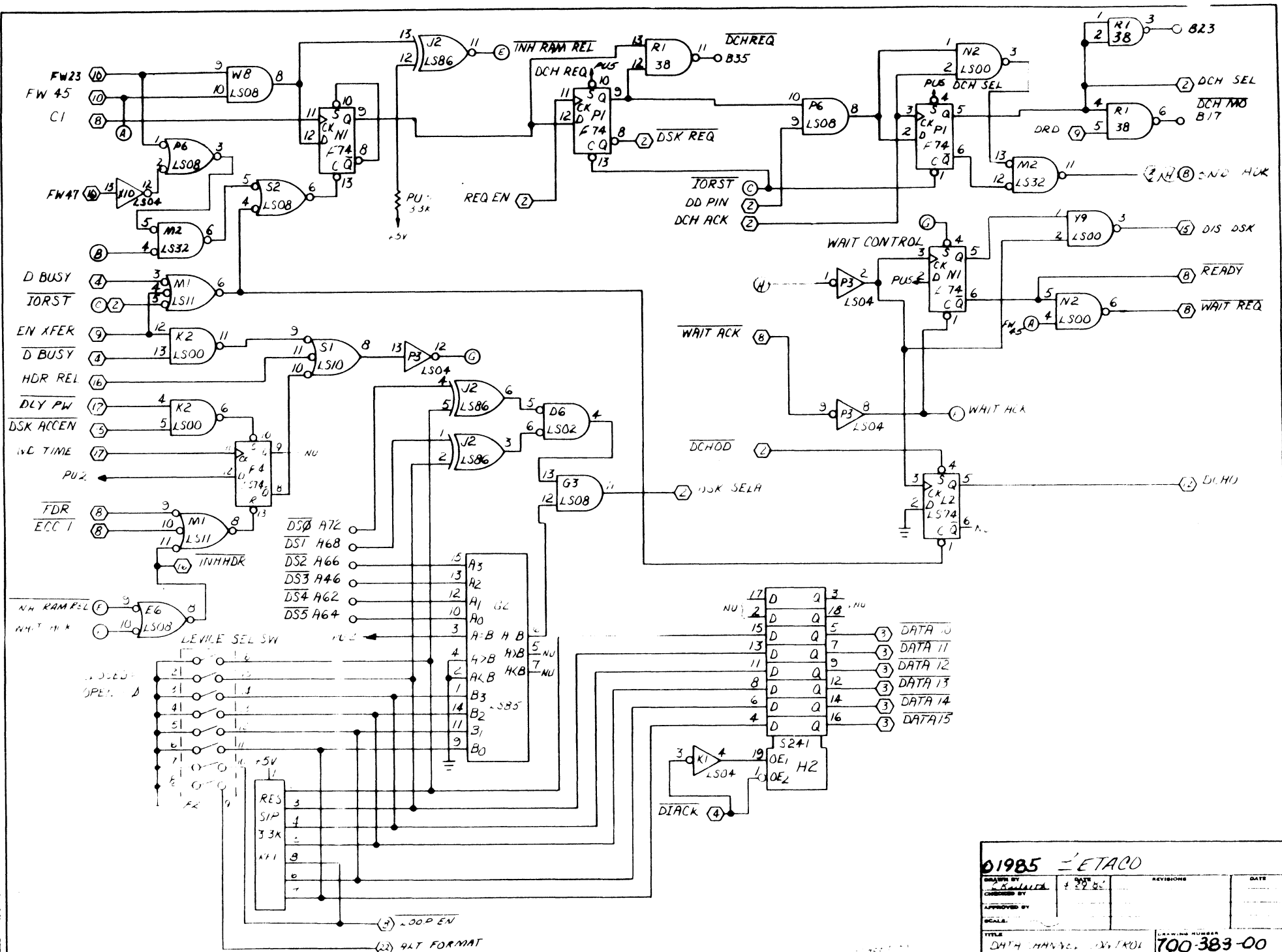
DATE	4-28-82	REVISED	
DESIGNED BY			
CONVERTED BY			
FILE NO.			
DCH DR/REC & ADDR GEN		700-33900.C	



**01985 ZETACO**

DATE	BY	REVISIONS	DATE
1/18/82	J.P.M.		
TITLE		DRAWING NUMBER	
DB PROGRAM CONTROL		700-383-00C	

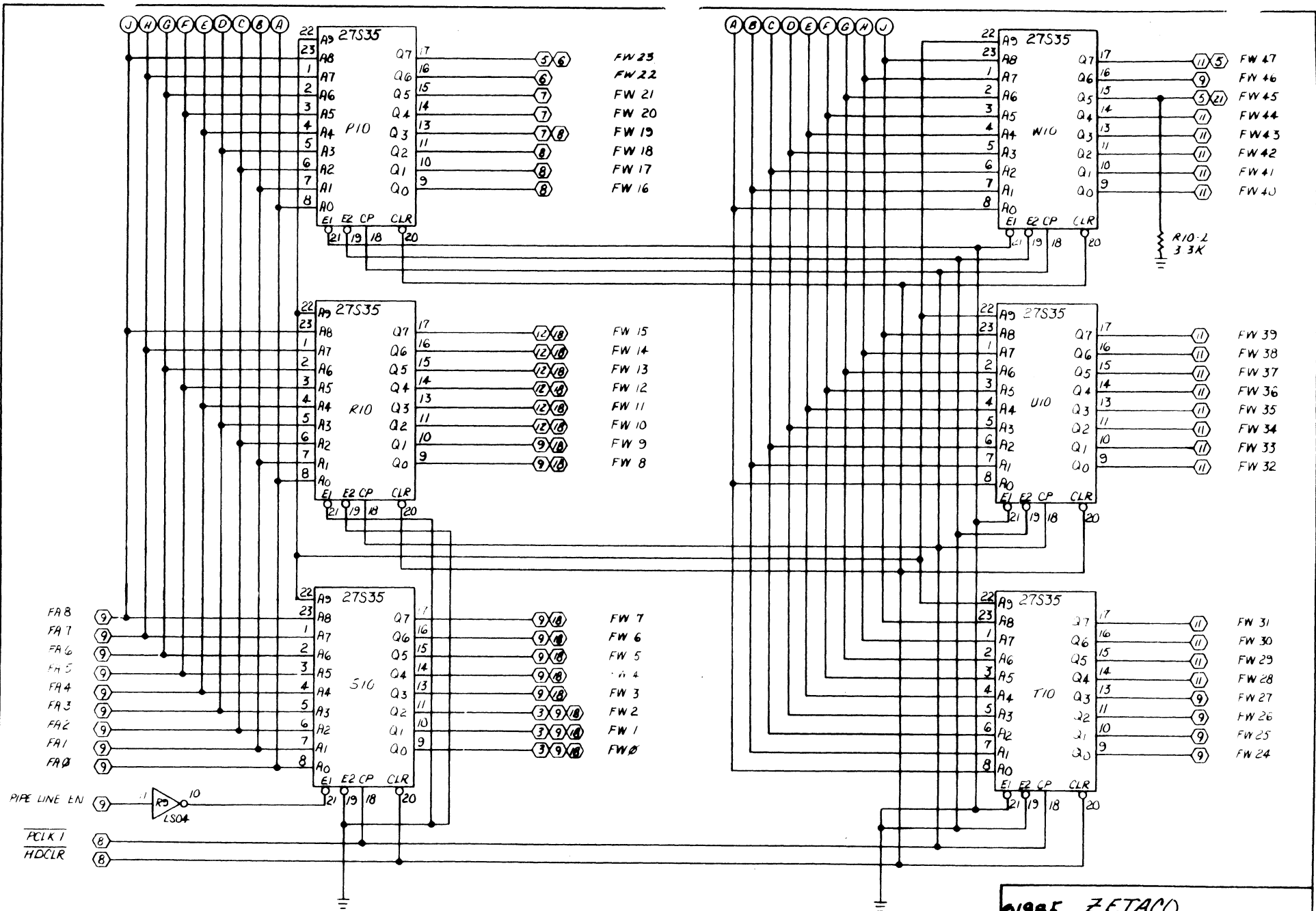
700383-000B



700383-000B

01985 - ETACO

DRAWN BY K. R. ...	DATE 4-29-61	REVISIONS	DATE
CHECKED BY			
APPROVED BY			
SCALE:			
TITLE DATA HANDLER CONTROL		DRAWING NUMBER 700-383-00	

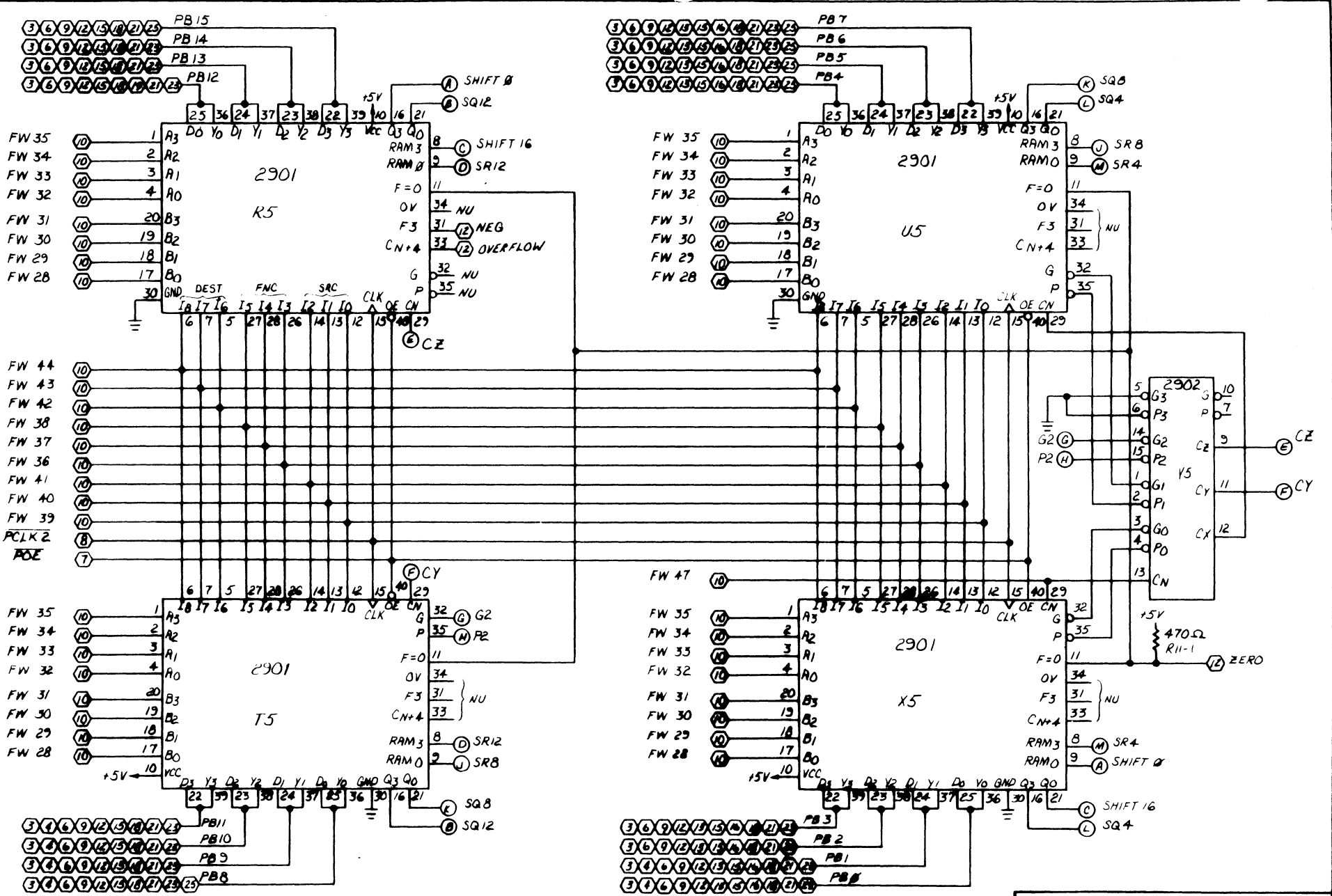


01985 ZETACO

DESIGNED BY	DATE	REVISIONS	DATE
APPROVED BY			
SCALE:			
TITLE	DRAWING NUMBER		
FIRMWARE	700-383-00 C		

ISHEET 101

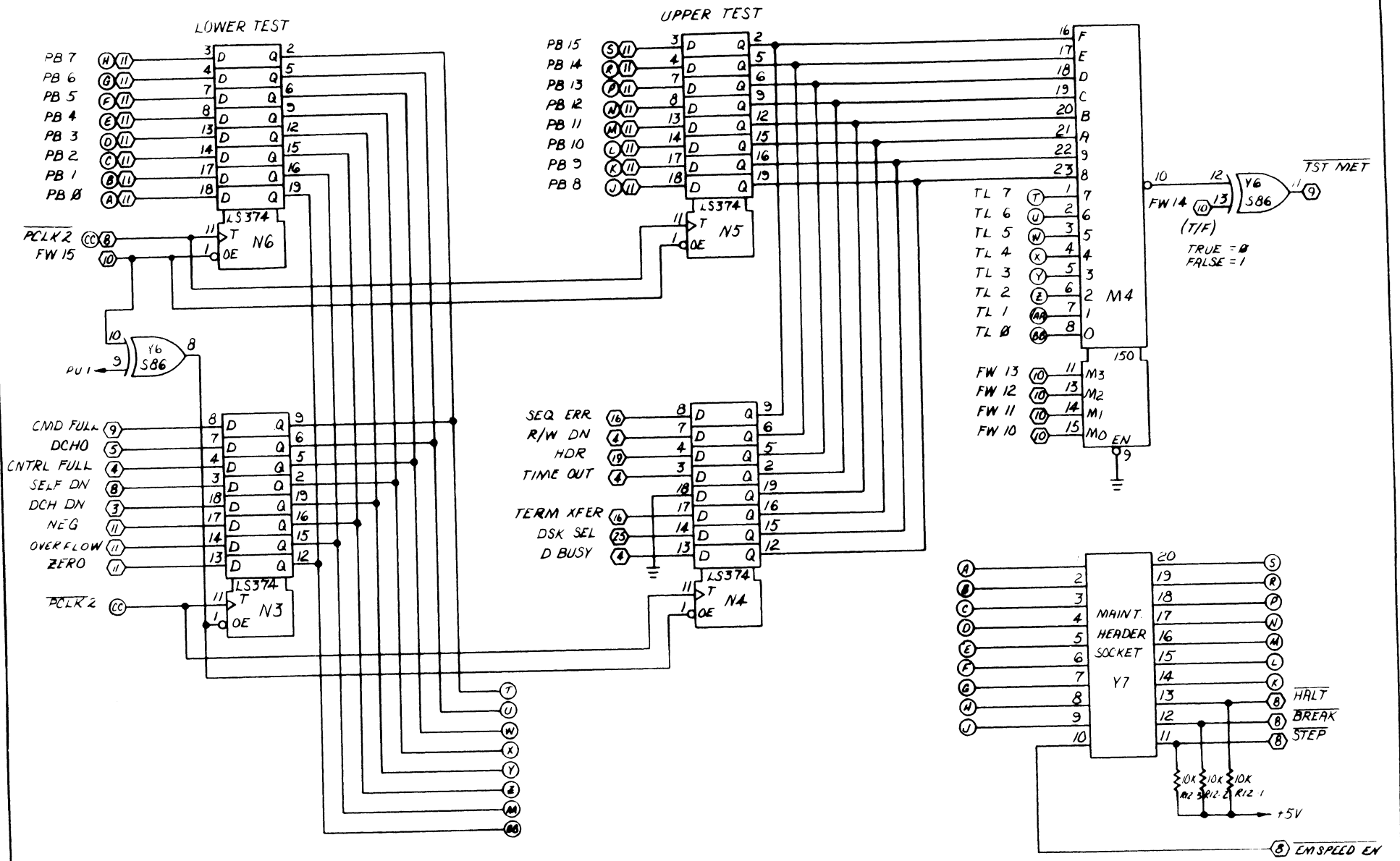
700383-0008



1985 ZETACO		REVISIONS	DATE
DESIGNED BY	4-29-82		
APPROVED BY			
DRAWN			
TITLE	PROCESSOR	QUANTITY NUMBER	700-383-00C

(SHEET 11)

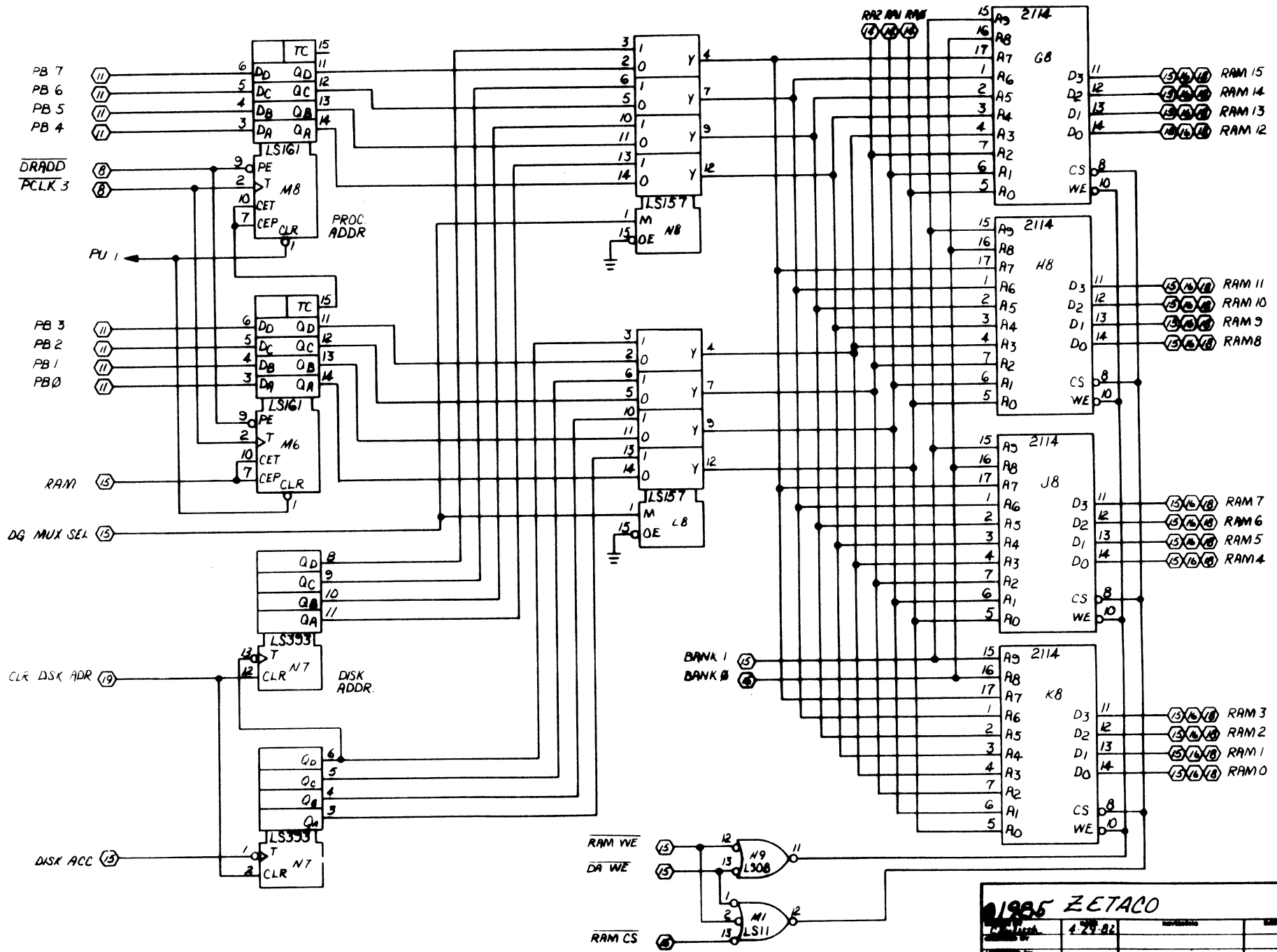
700383-000 B



91985 ZETACO		REVISION	DATE
DESIGNED BY	4 28 82		
DRAWN BY			
SCALE			
TITLE	TEST CONDITION	DRAWING NUMBER	700-383-00 C

(SHEET 12)

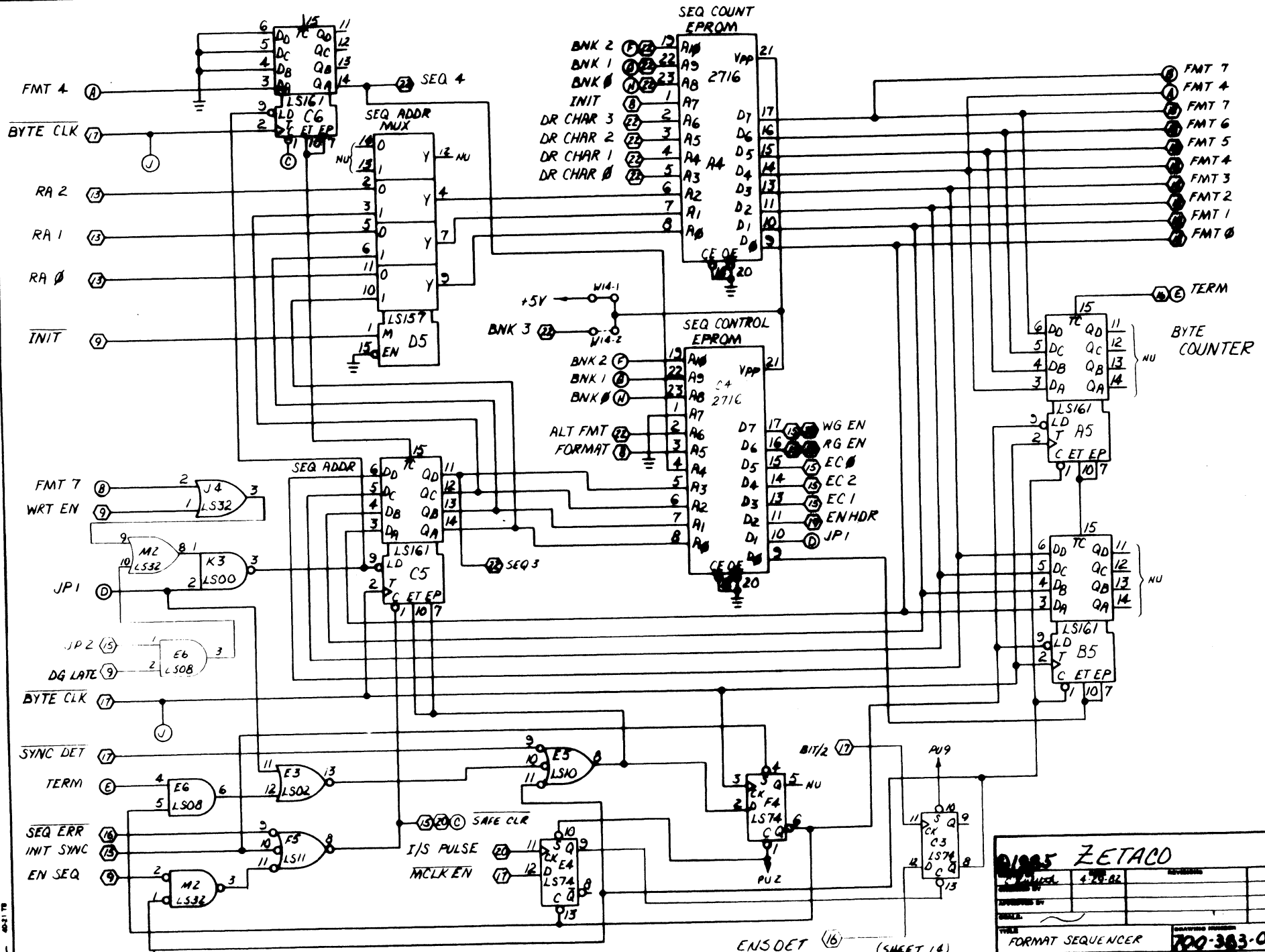




**1965 ZETACO**

DATE	4-29-62	REVISED	
DESIGNED BY		CHECKED	
APPROVED BY			
DRAWN			
TITLE	MEMORY		DISPATCH NUMBER
			700-303-00 C

40-2178



**ZETACO**

01005

4-78-02

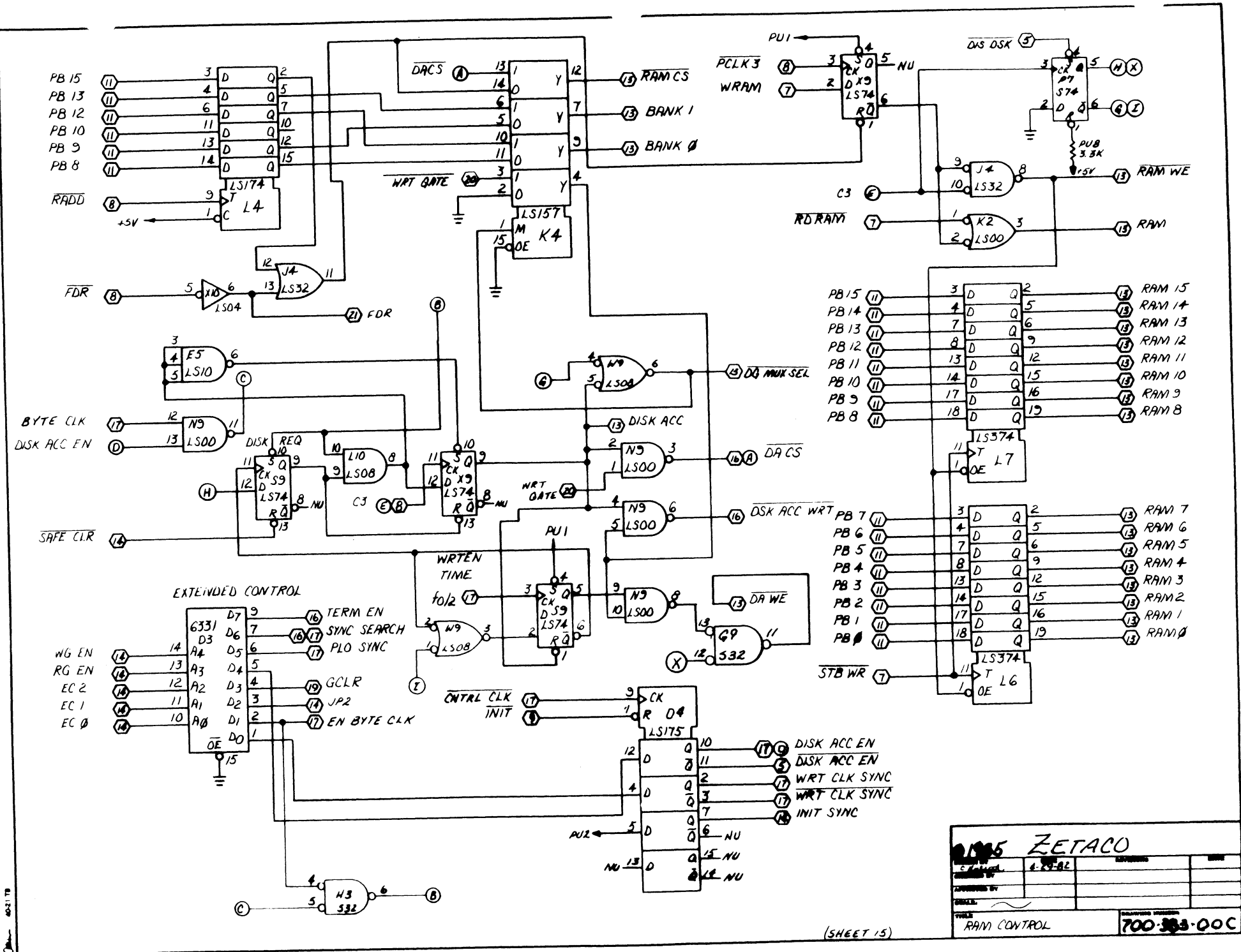
DATE: \_\_\_\_\_

DESIGNED BY: \_\_\_\_\_

DRAWN BY: \_\_\_\_\_

FILE: **FORMAT SEQUENCER**

700-383-00C

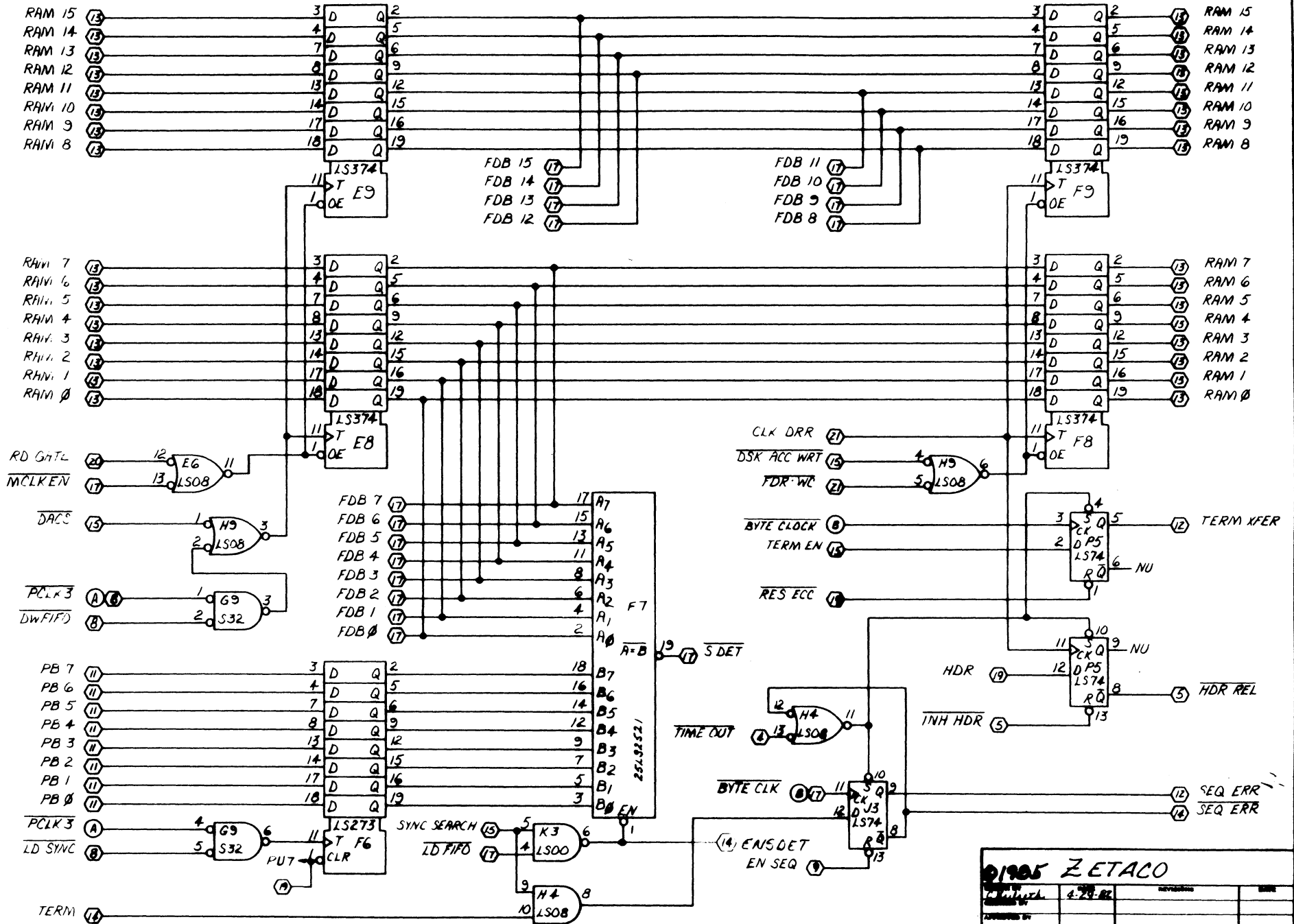


700383-000B

(SHEET 15)

<p><b>ZETACO</b></p>	
<p>DATE: 4-22-82</p>	<p>DESIGNED BY:</p>
<p>APPROVED BY:</p>	<p>DATE:</p>
<p>TITLE: RAM CONTROL</p>	<p>PROJECT NUMBER: 700-383-000</p>

DISK WRITE REG

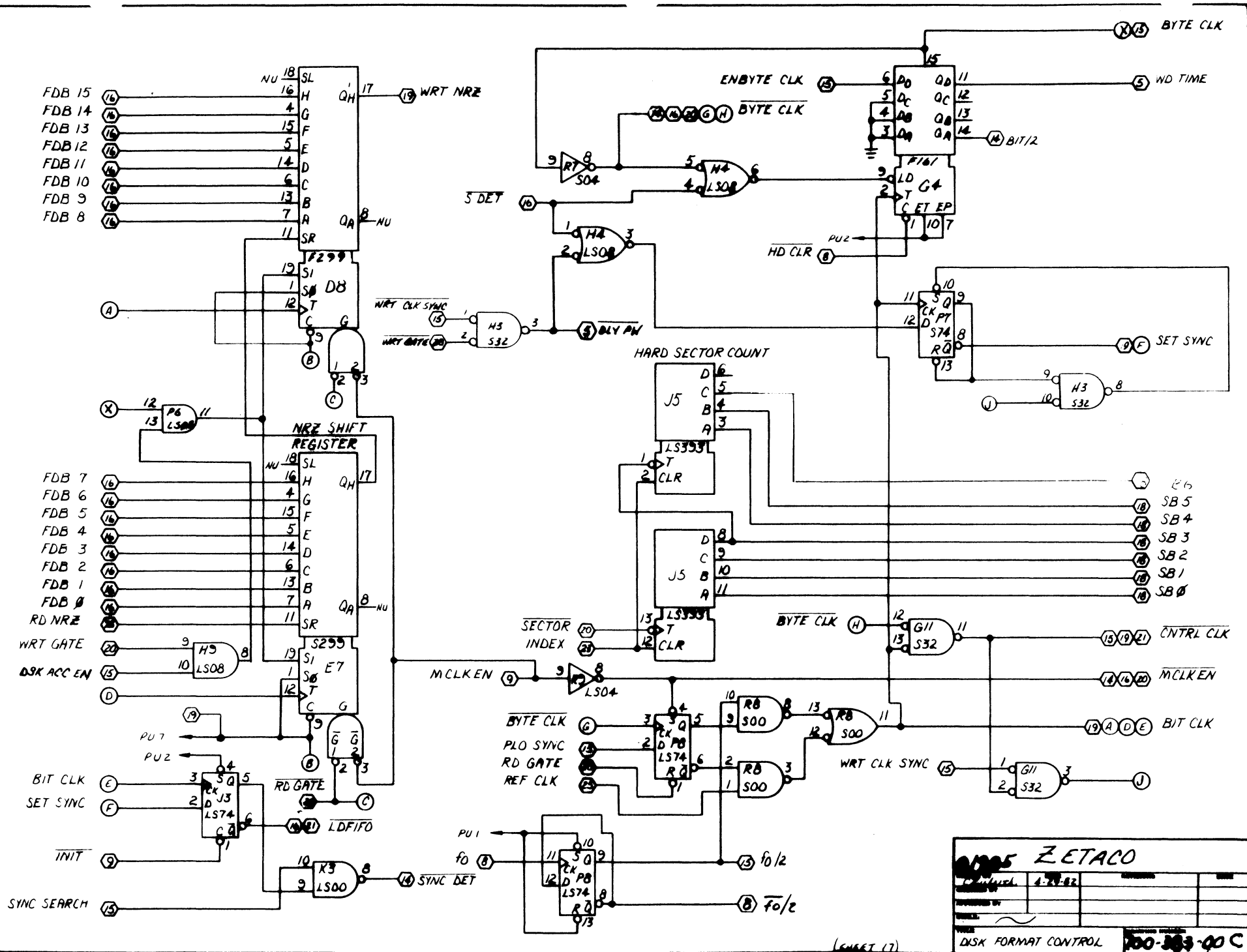


**01905 ZETACO**

DATE	4-24-82	REVISION	
APPROVED BY			
DRAWN			
TITLE SYNC DET AND FORMAT BUS REG			
			700-383-00 C

(SHEET 16)

700383-000 B



**ZETACO**

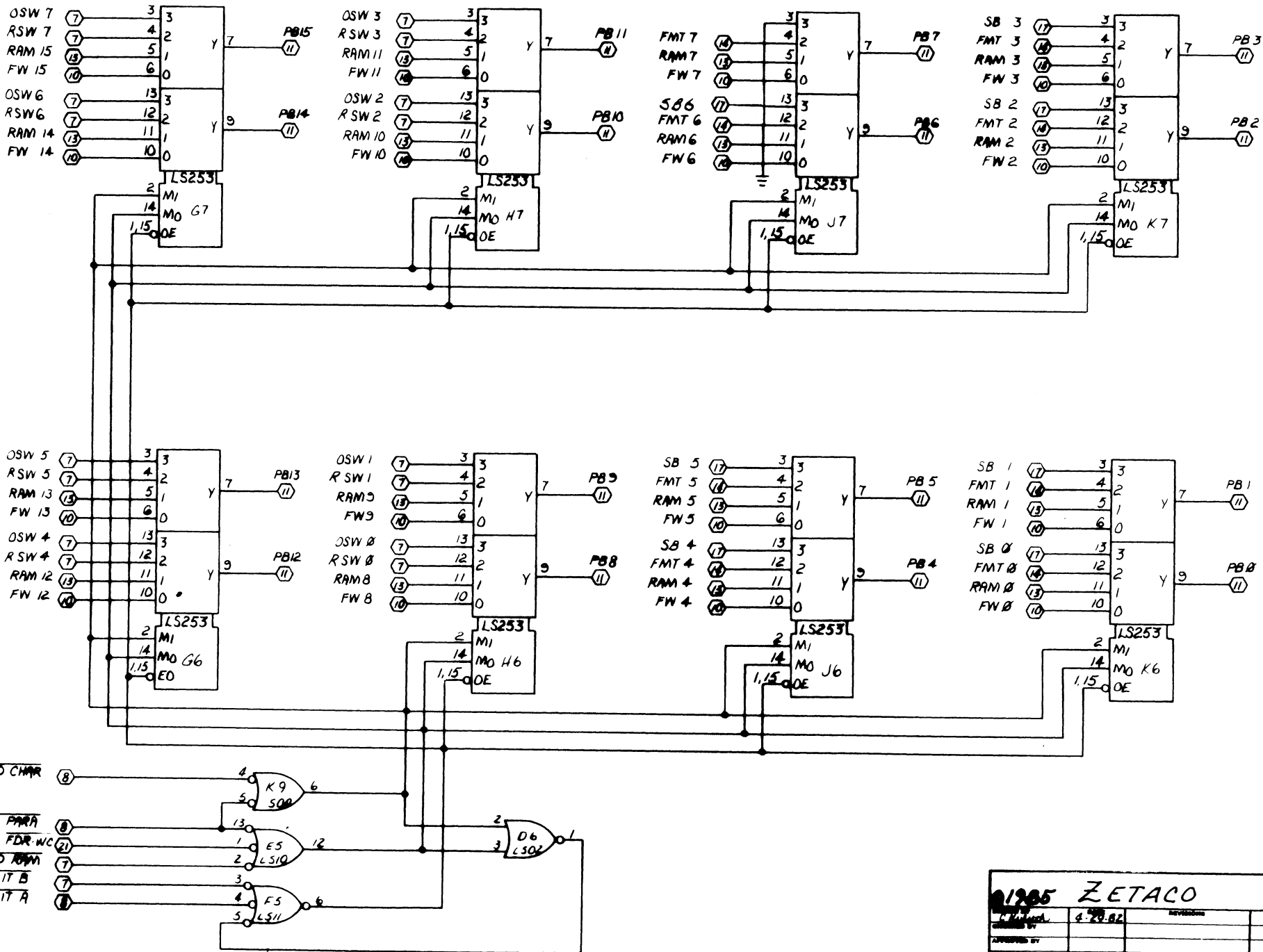
4-78-82

DISK FORMAT CONTROL

700-383-00C

700383-0008

(SHEET 17)

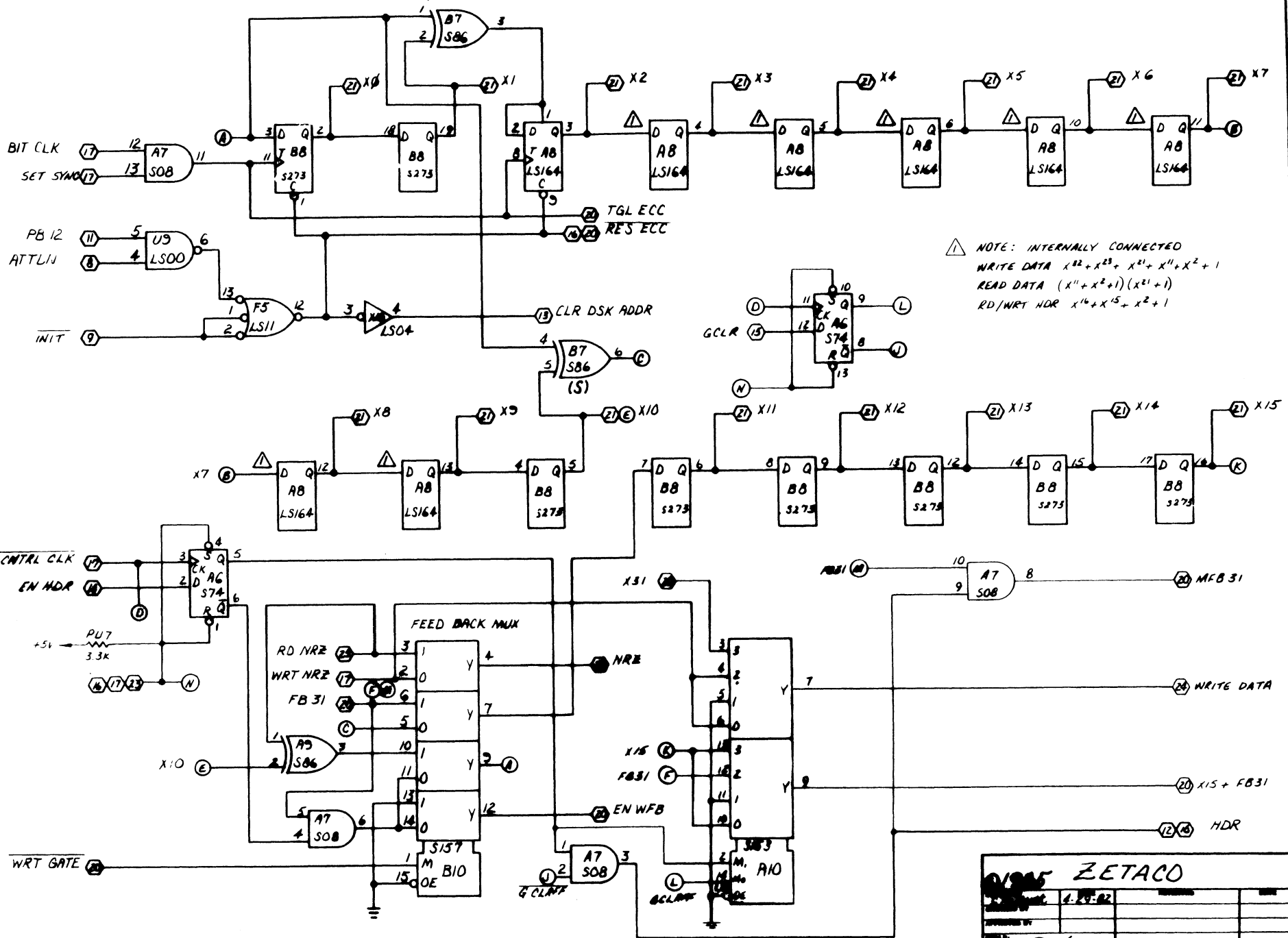


21985 ZETACO			
DATE	4-29-82	REVISION	
DESIGNED BY			
CHECKED BY			
DRAWING NUMBER	700-303-00 C		
PB READ MUX			

(SHEET 18)

700303-000 B

40-2178



**ZETACO**

DATE: 1-24-82

DESIGNED BY: \_\_\_\_\_

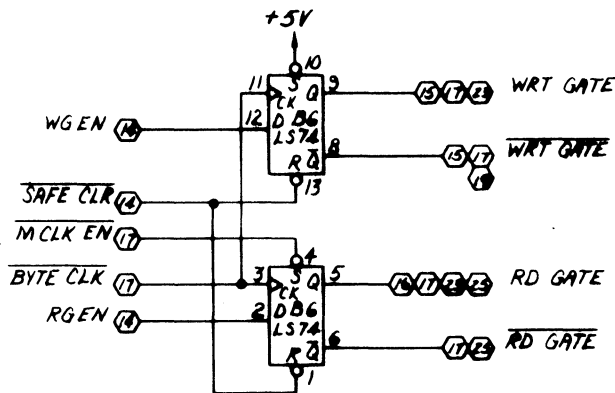
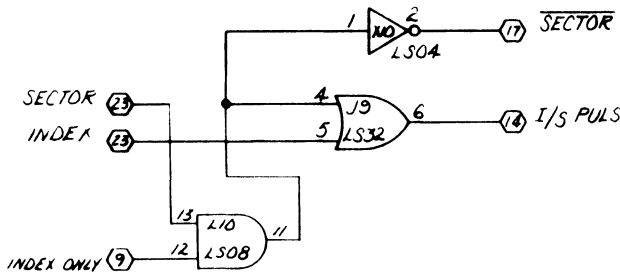
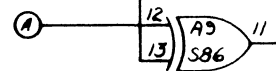
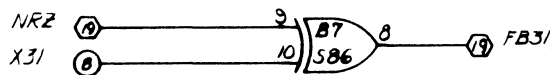
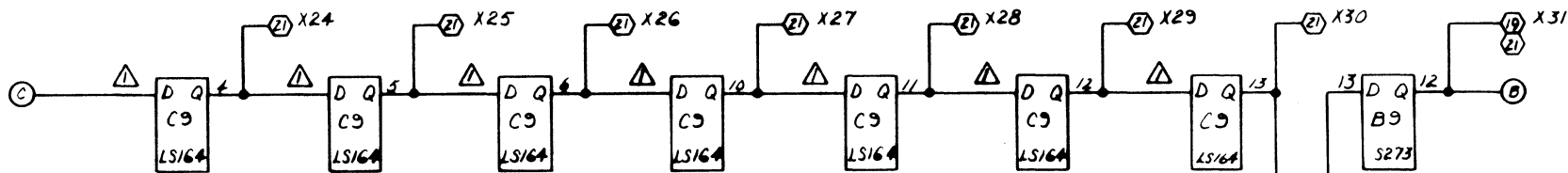
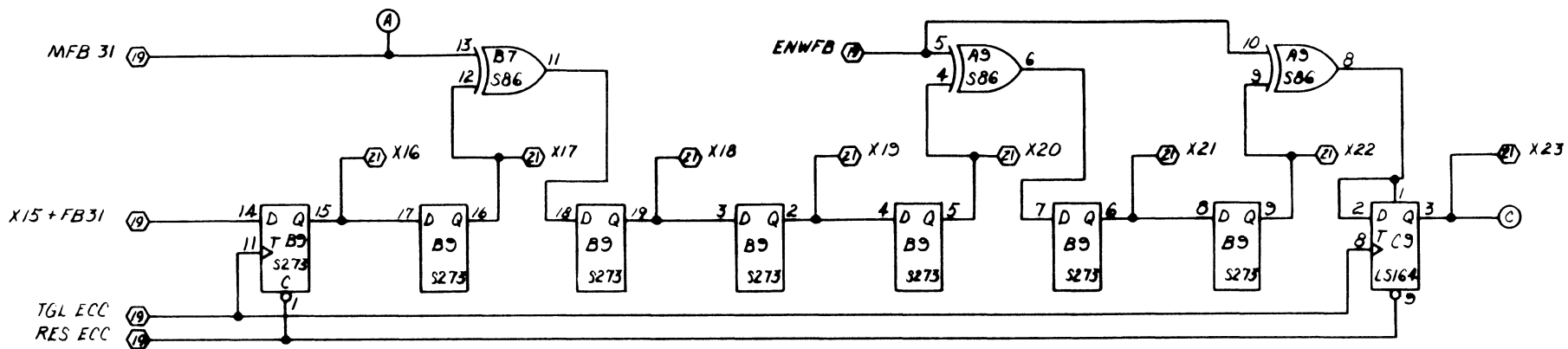
DRAWN BY: \_\_\_\_\_

WILL: \_\_\_\_\_

WAVE: \_\_\_\_\_

ECC LOWER

700-383-00C

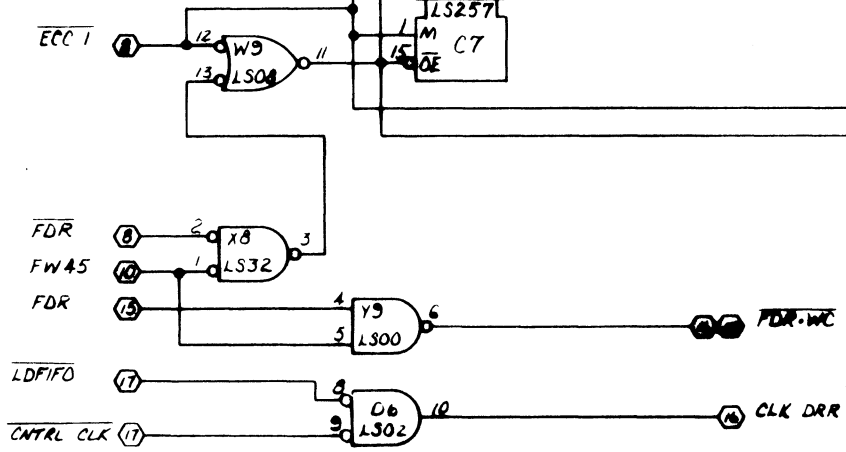
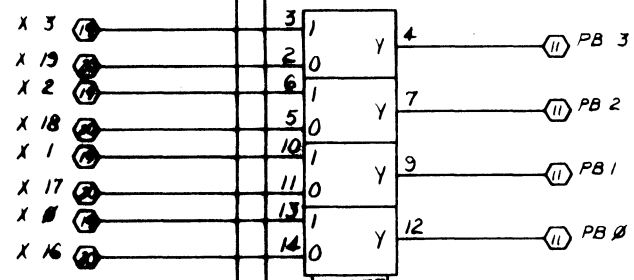
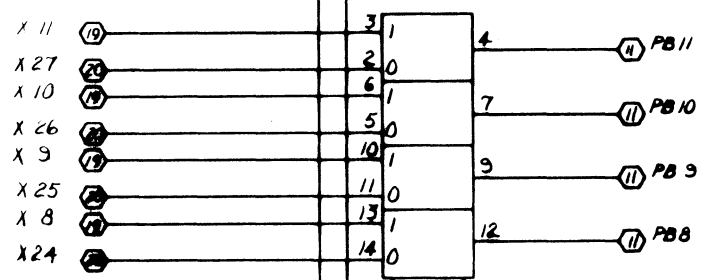
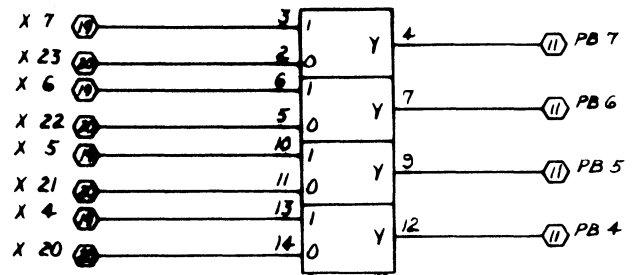
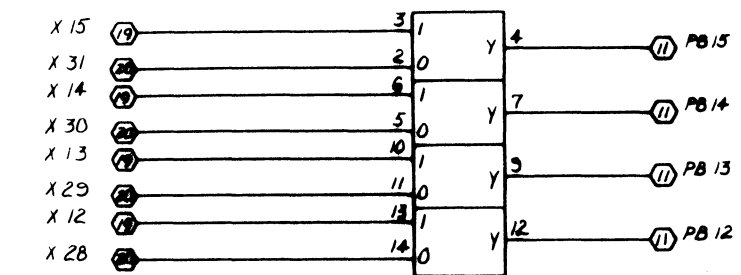


△ NOTE: INTERNALLY CONNECTED

21925 ZETACO		REVISED	DATE
DESIGNED BY	1-21-82		
APPROVED BY			
TITLE			
700393-000 B	DRAWING NUMBER		700-393-00 C

(SHEET 20)

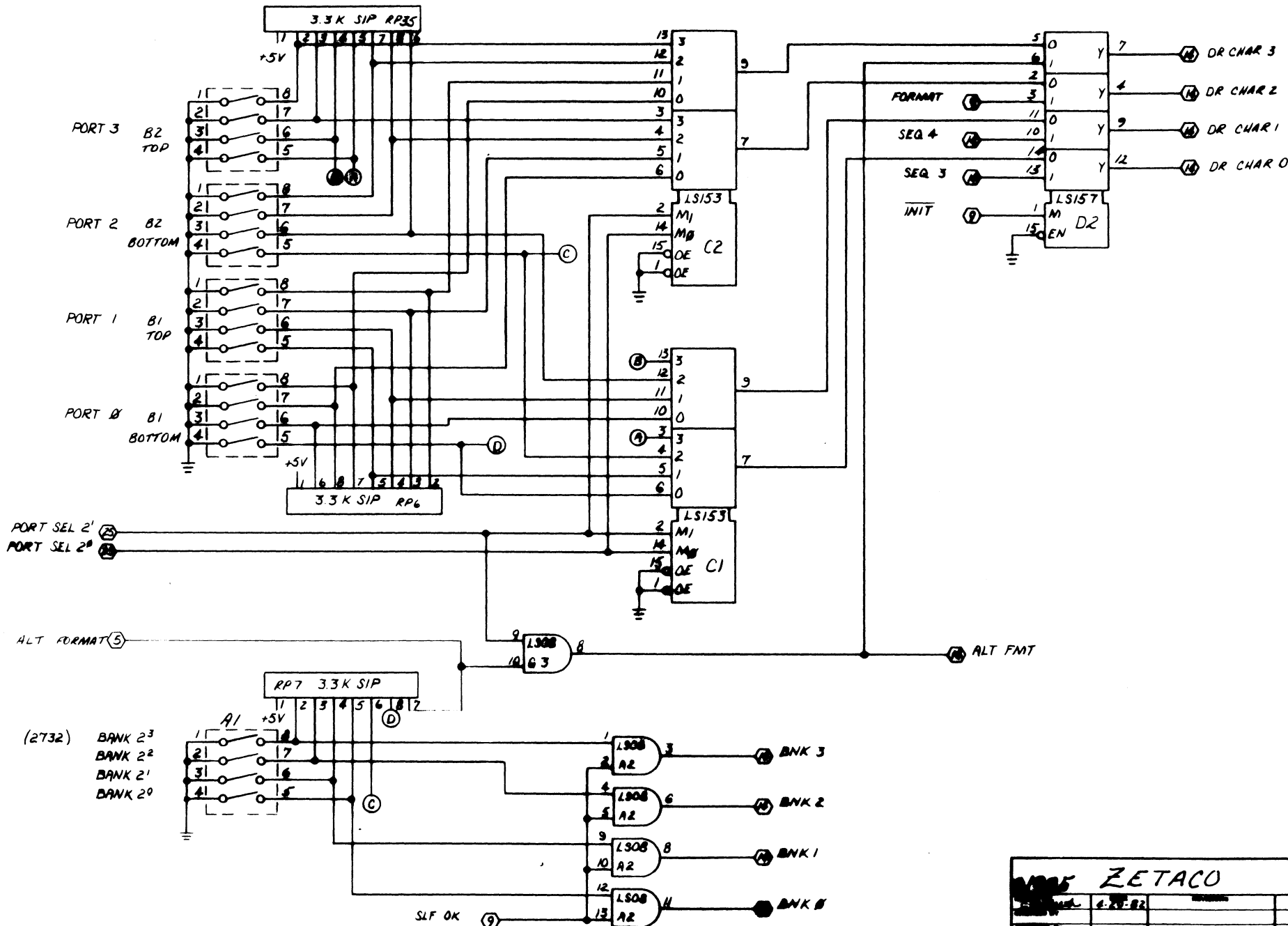




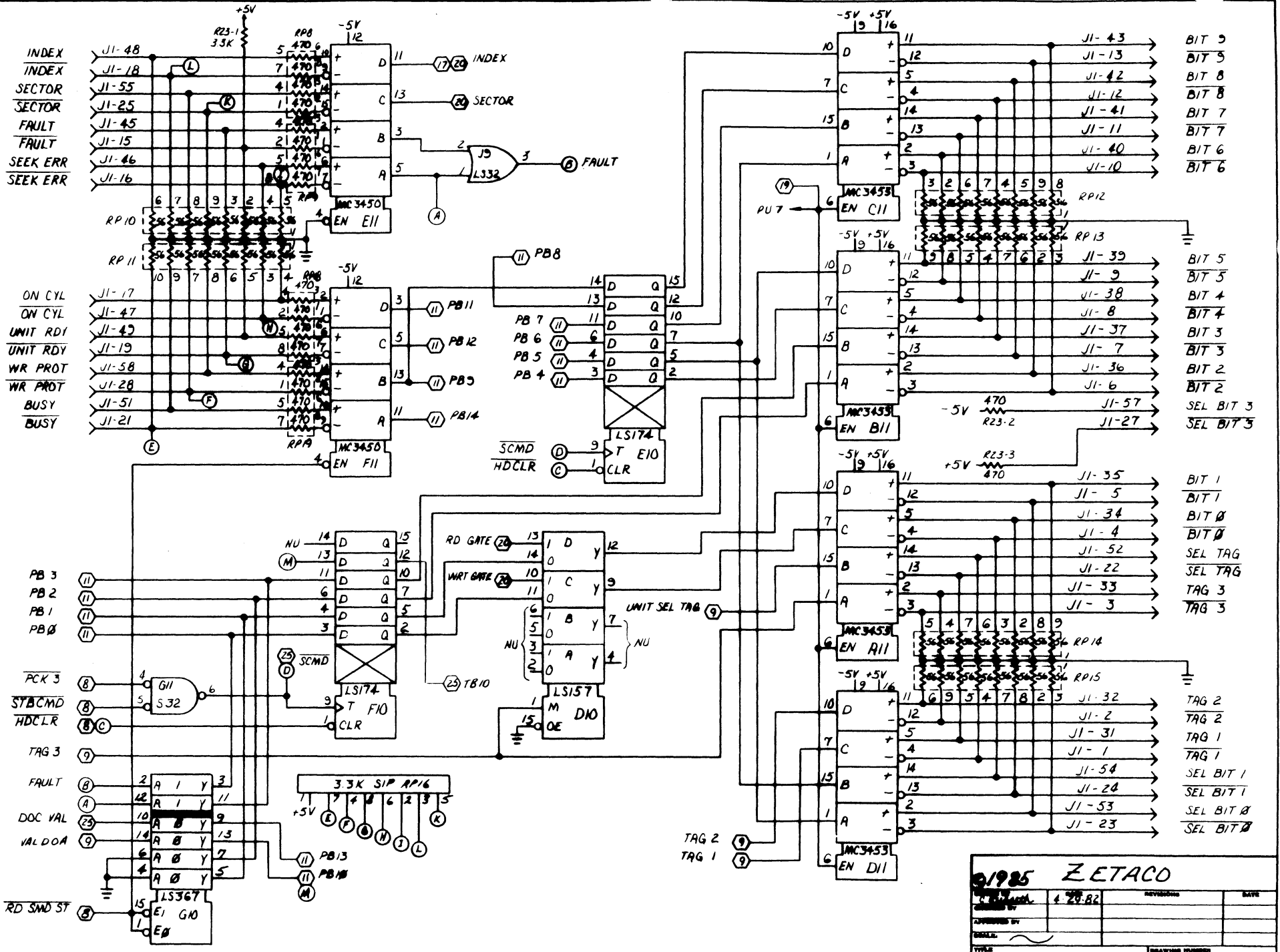
1985 ZETACO

DATE	4-29-82	REVISION	
APPROVED BY			
ECC OUTPUT SELECT			

700-303-00 C

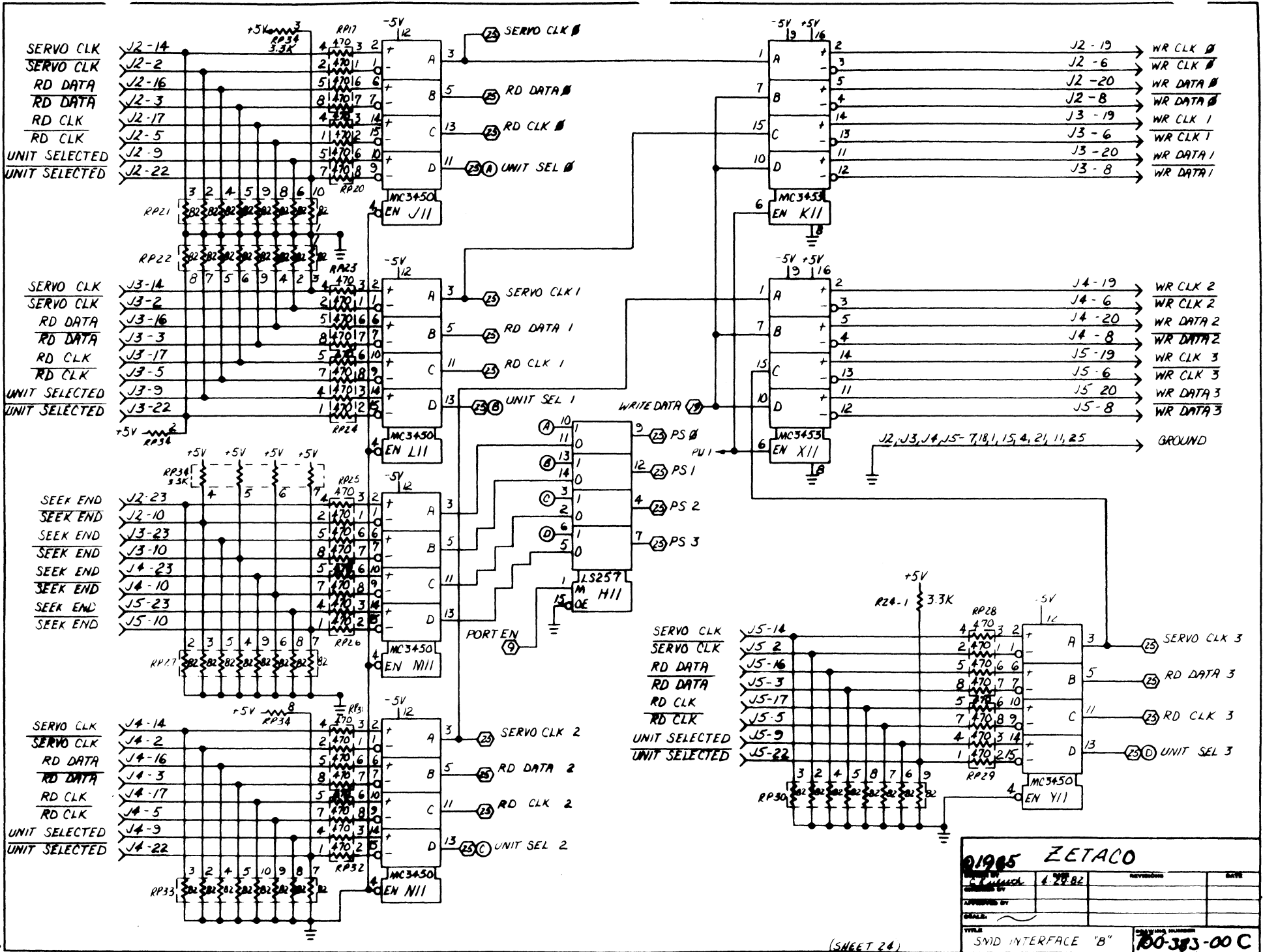


ZETACO			
DATE	4-28-82	DESIGNED BY	
APPROVED BY		TESTED BY	
TITLE		PART NUMBER	
FORMAT BANK SELECT		700-383-00 C	



01985 ZETACO

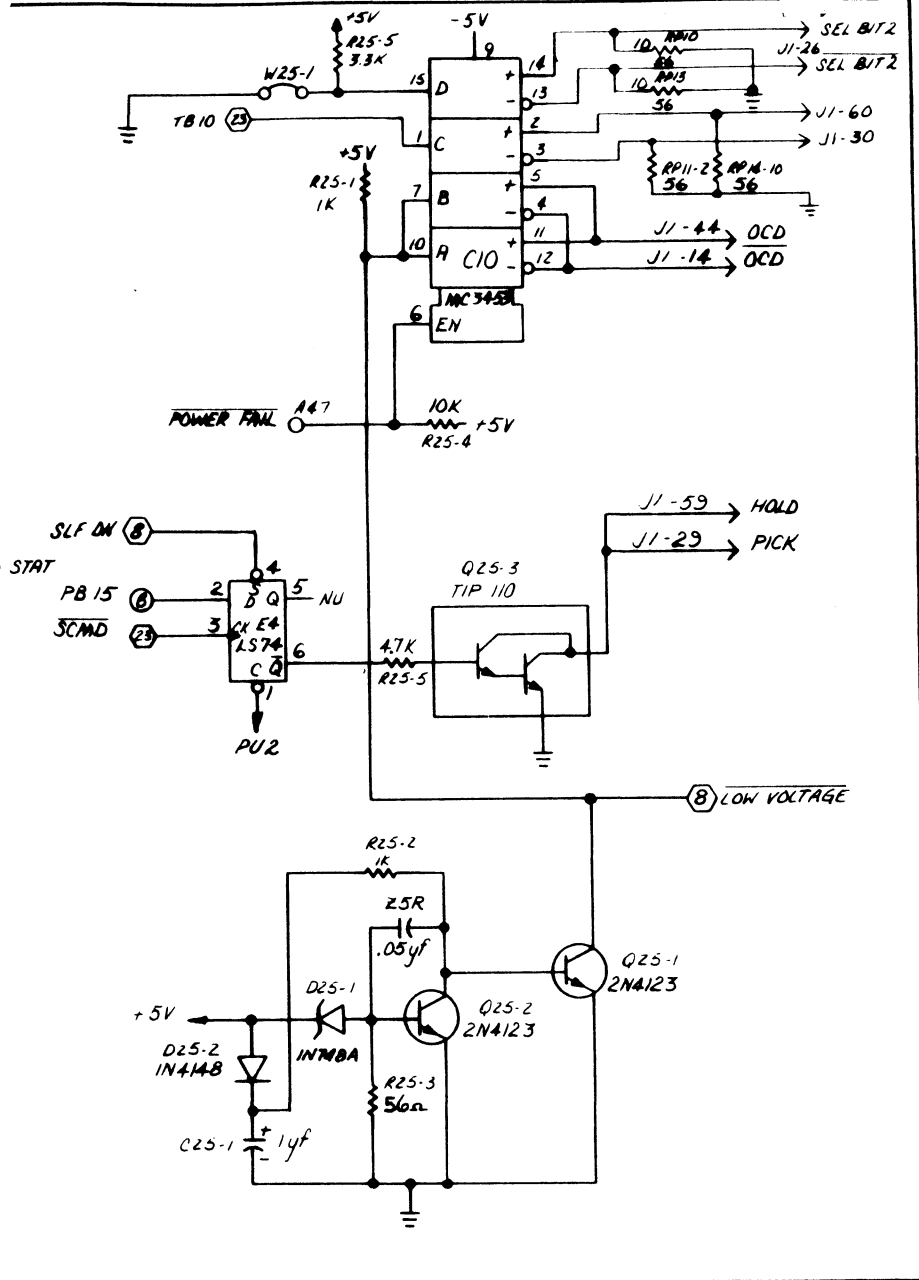
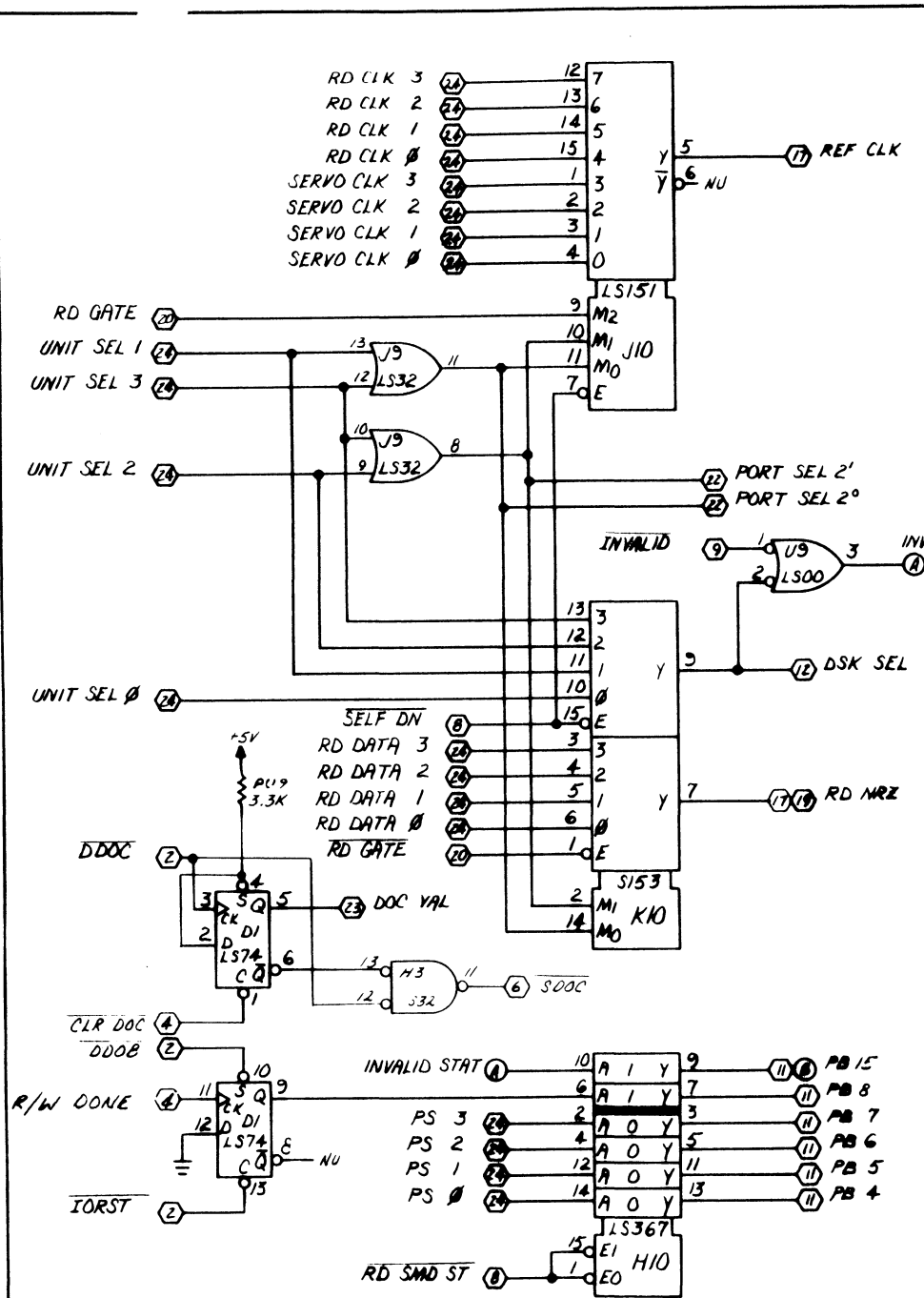
DATE	4-29-82	REVISIONS	DATE
DESIGNED BY			
CHECKED BY			
DATE			
TITLE	SMD INTERFACE 'A'		QUANTITY ORDERED
			700-383-00C



**ZETACO**

DATE	4.29.82	REVISIONS	DATE
DESIGNED BY			
CHECKED BY			
DRAWN BY			
TITLE	SMD INTERFACE "B"		DRAWING NUMBER
			100-383-00 C

700383-000 B



1985 ZETACO  
 DESIGNED BY: [Signature] 4-28-82  
 CHECKED BY: [Signature]  
 APPROVED BY: [Signature]  
 TITLE: SMD INTERFACE "CONTRAC" 700-383-00C

700383-000 B

REVISION HISTORY		
ECO	DATE	DESCRIPTION
0096	2-22-83	SHEETS 5, 15, 17, 25 AFFECTED
0103	3-10-83	CORRECT SCHEMATICS
0148	6-6-83	SHEETS 2 & 8
0149	6-16-83	SHEETS 4 & 9
0217	1-4-84	SHEET 17 & 20
0258	3-13-84	SHEETS 8, 15, 17, 19, 20, 25
0283	3-30-84	SHEET 4
0336	6-29-84	SHEETS 4, 5, 8, 14, 16, 17, 22, 25,
0376	9-0-84	SHEET 17 & 18
0418	12-7-84	SHEETS 4 & 5
0511	10-85	SHEET 25

DC-295C

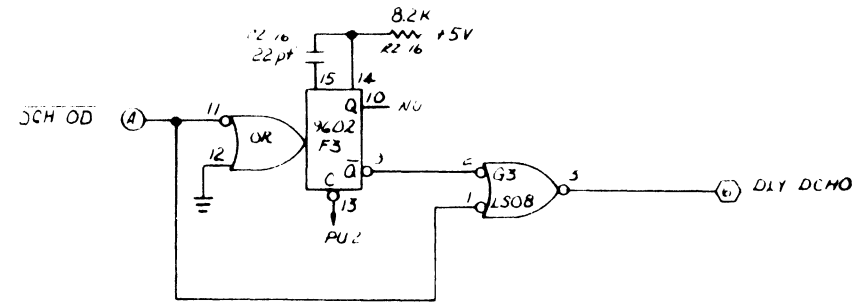
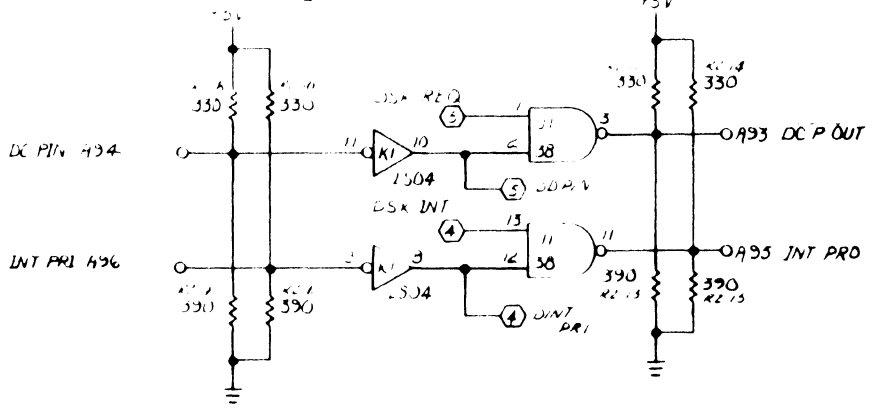
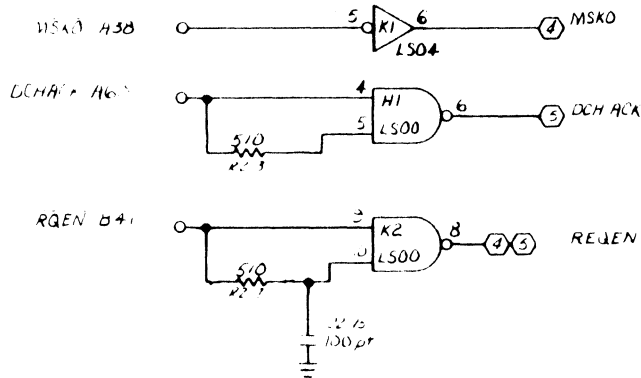
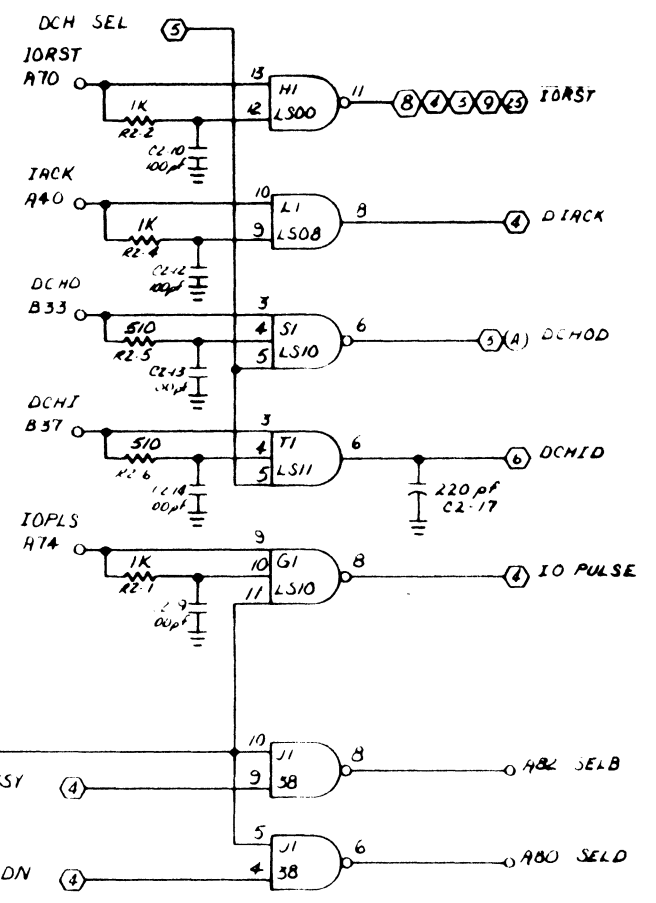
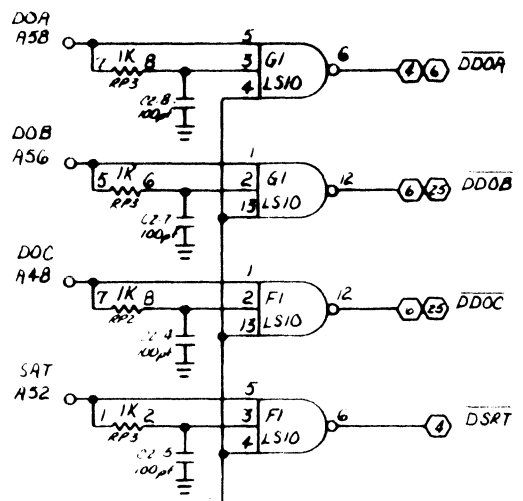
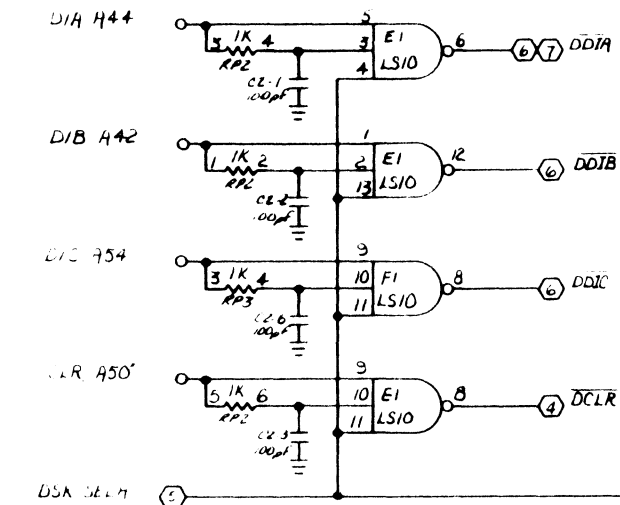
NOTE:

1. NUMBERS FOUND WITHIN THE HEXAGON SYMBOLS INDICATES SHEETS WHERE CONTINUED LOGIC WILL BE FOUND  
 EXAMPLE (2) = SHEET 2

(SHEET 1 OF 25)

ZETACO			
DATE	BY	REVISION	DESCRIPTION
DC-295C		700-383-0008	

700383-0008

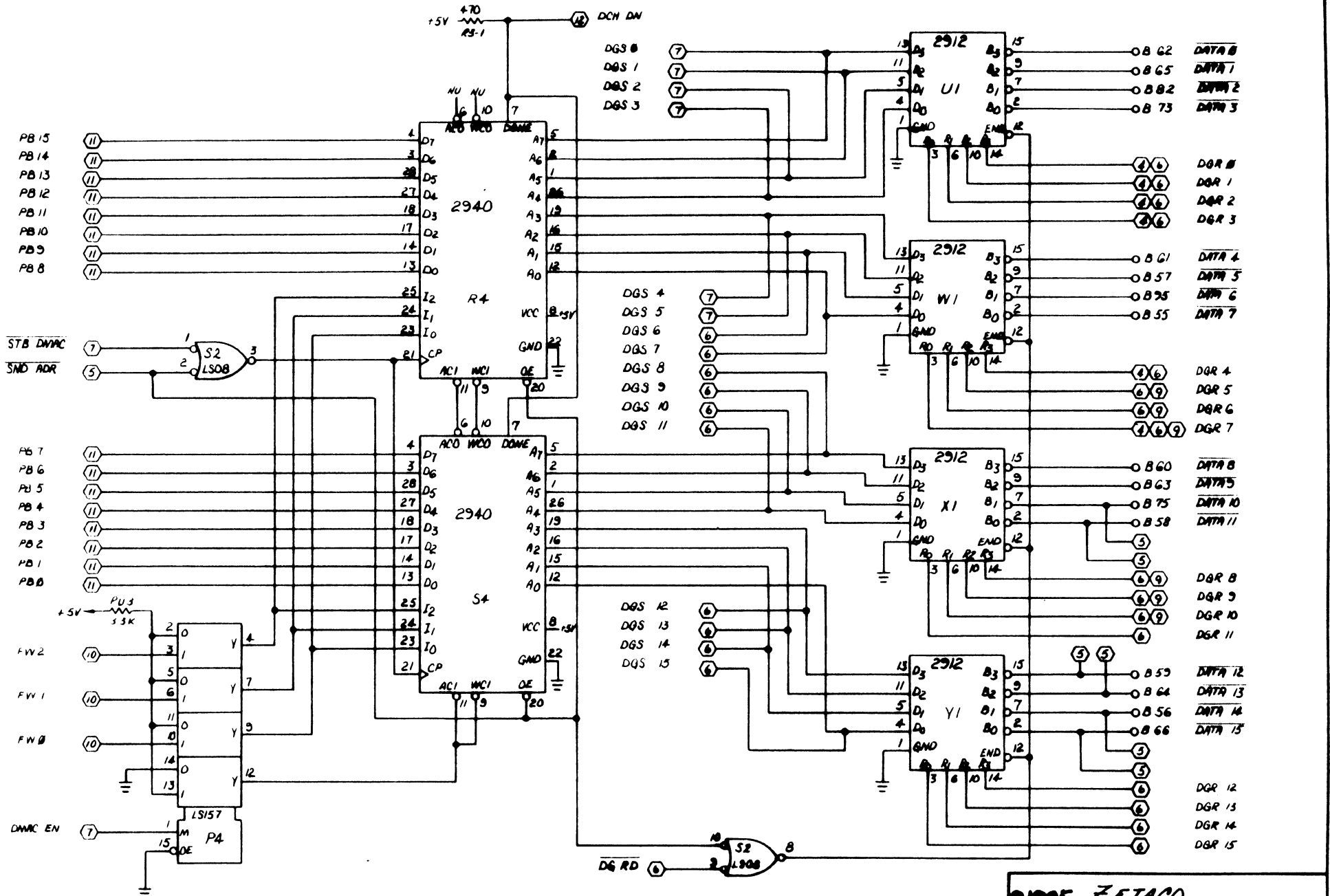


(SHEET 2)

**1985 ZETACO**

DESIGNED BY	DATE	REVISED BY	REVISED DATE
C. MULLA	4/29/85		
CHECKED BY			
APPROVED BY			
DATE			
TITLE		DRAWING NUMBER	
DG INTERFACE		700-383-00	

700383-000B



PB 15  
PB 14  
PB 13  
PB 12  
PB 11  
PB 10  
PB 9  
PB 8

STB DMAC  
SND ADR

PB 7  
PB 6  
PB 5  
PB 4  
PB 3  
PB 2  
PB 1  
PB 0

FW 2  
FW 1  
FW 0

DMAC EN

DGS 0  
DGS 1  
DGS 2  
DGS 3

DGS 4  
DGS 5  
DGS 6  
DGS 7  
DGS 8  
DGS 9  
DGS 10  
DGS 11

DGS 12  
DGS 13  
DGS 14  
DGS 15

DATA 0  
DATA 1  
DATA 2  
DATA 3

DGR 0  
DGR 1  
DGR 2  
DGR 3

DATA 4  
DATA 5  
DATA 6  
DATA 7

DGR 4  
DGR 5  
DGR 6  
DGR 7

DATA 8  
DATA 9  
DATA 10  
DATA 11

DGR 8  
DGR 9  
DGR 10  
DGR 11

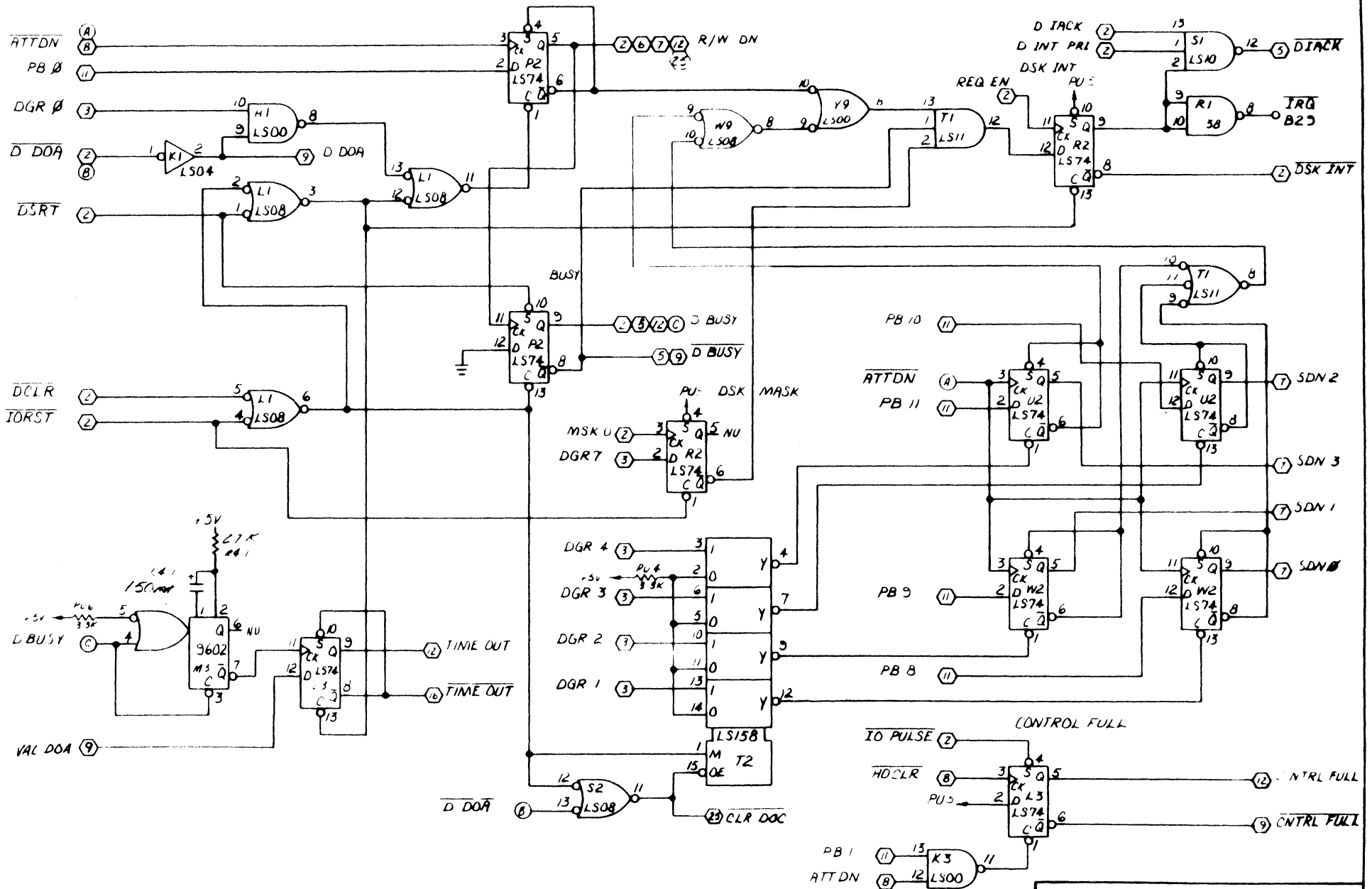
DATA 12  
DATA 13  
DATA 14  
DATA 15

DGR 12  
DGR 13  
DGR 14  
DGR 15

**2195 ZETACO**

DATE	6-1982
DESIGNED BY	
CHECKED BY	
DATE	
DCH DR/REC & ADDR GEN	
100-33900.C	





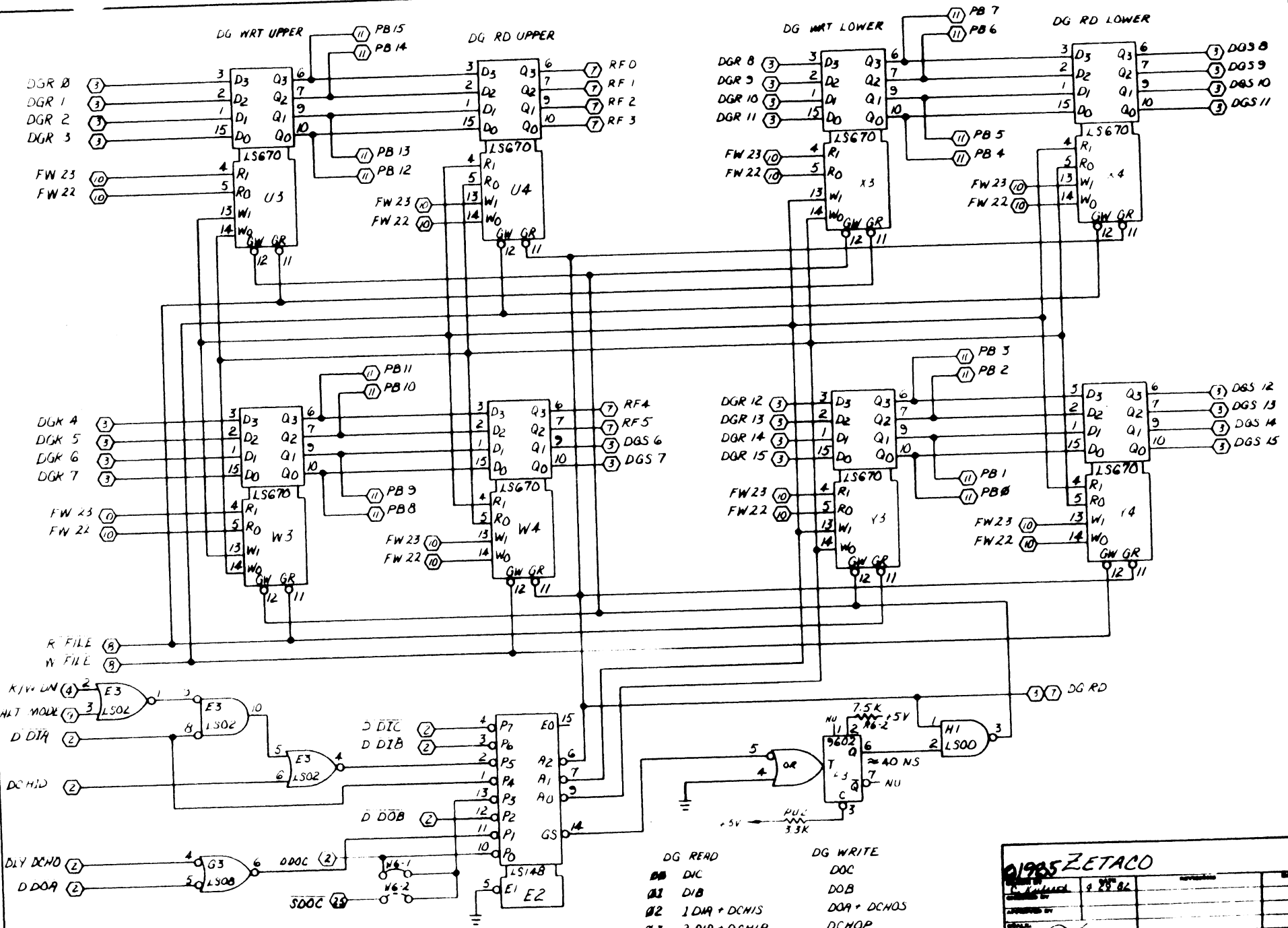
1985 ZETACO

DATE	4/28/84	REVISION	
DESIGNED BY		APPROVED BY	
CHECKED BY		DATE	
TITLE		DRAWING NUMBER	
DG PROGRAM CONTROL		700-385-006	

700383-000B

12447 4/

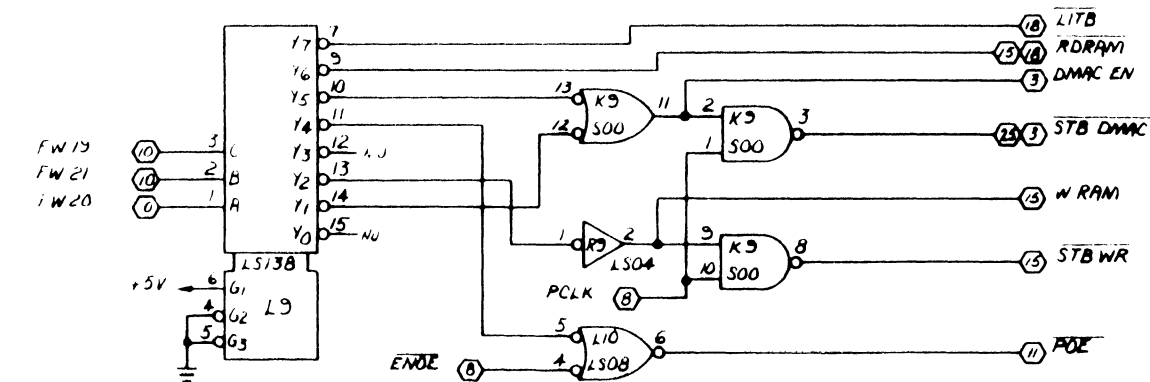
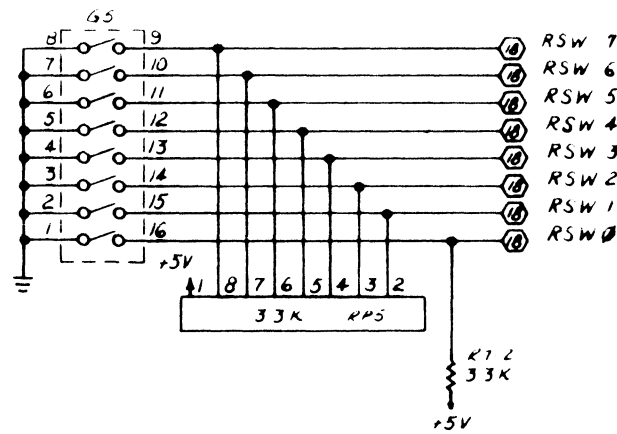
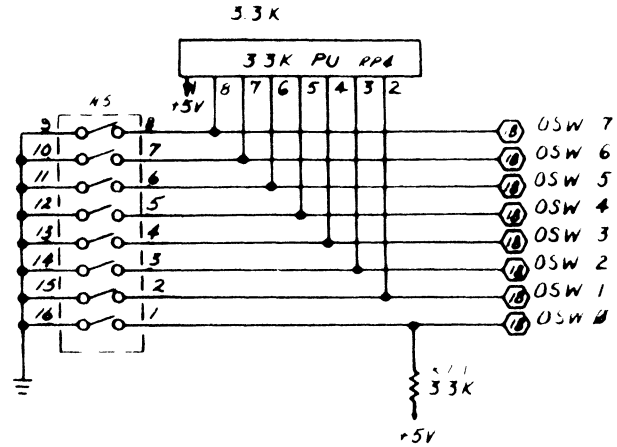
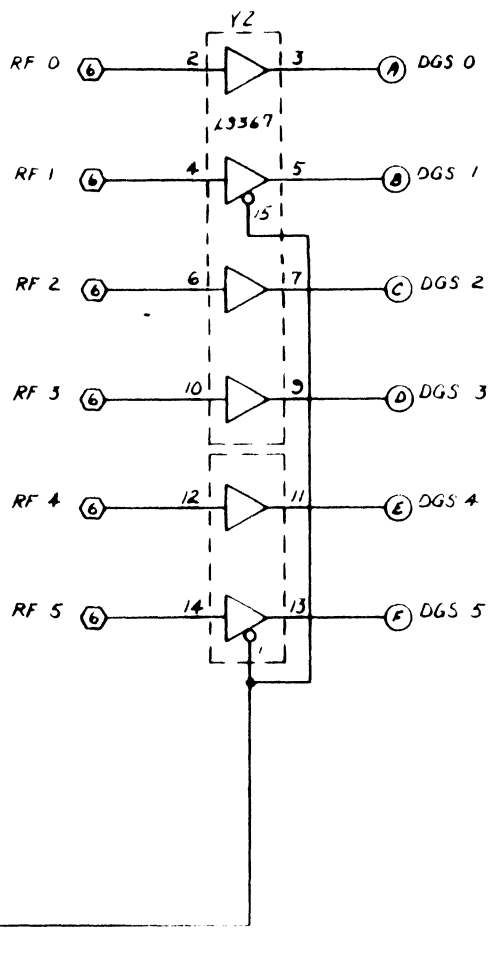
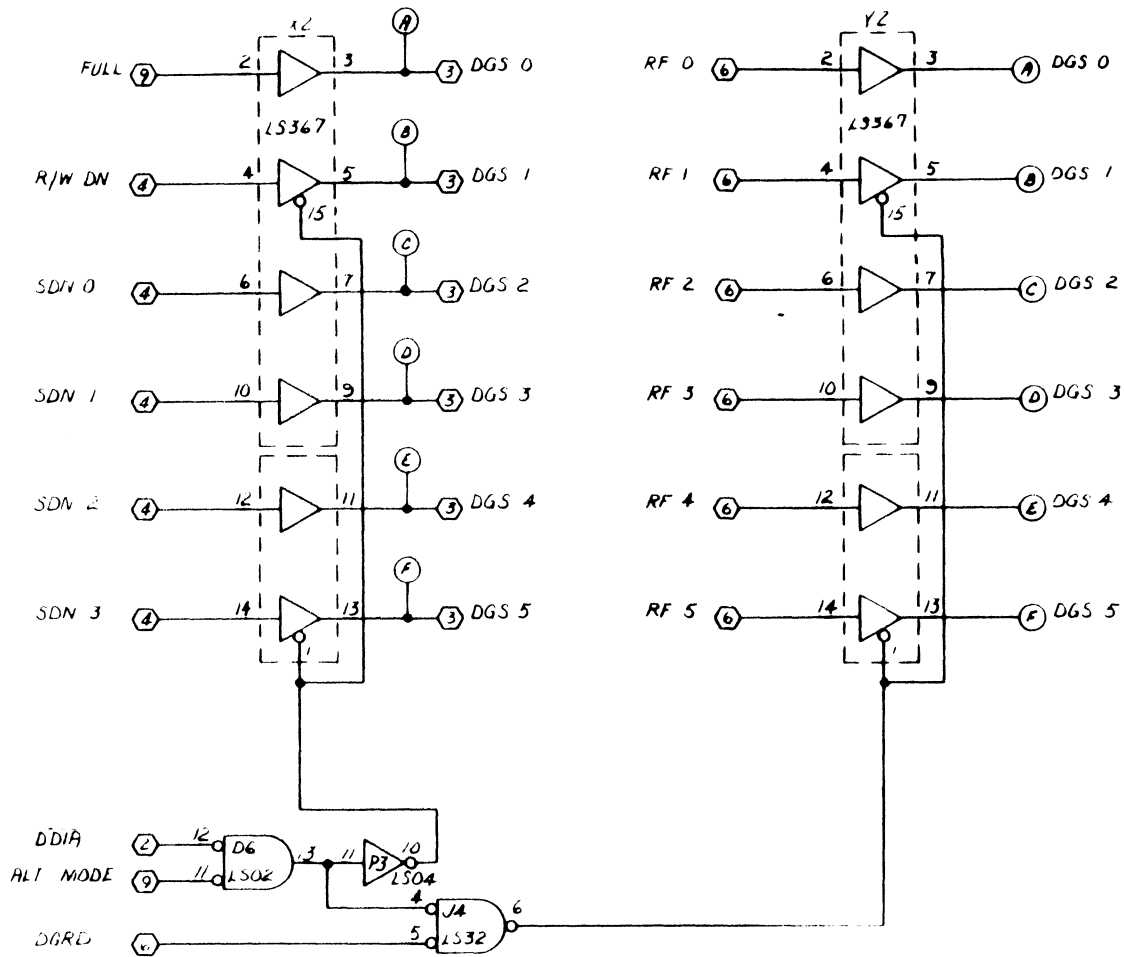




DG READ  
 00 DIC  
 01 DIB  
 02 1 DWA + DCHIS  
 03 2 DIA + DCHIP

DG WRITE  
 00C  
 00B  
 00A + DCHOS  
 DCHOP

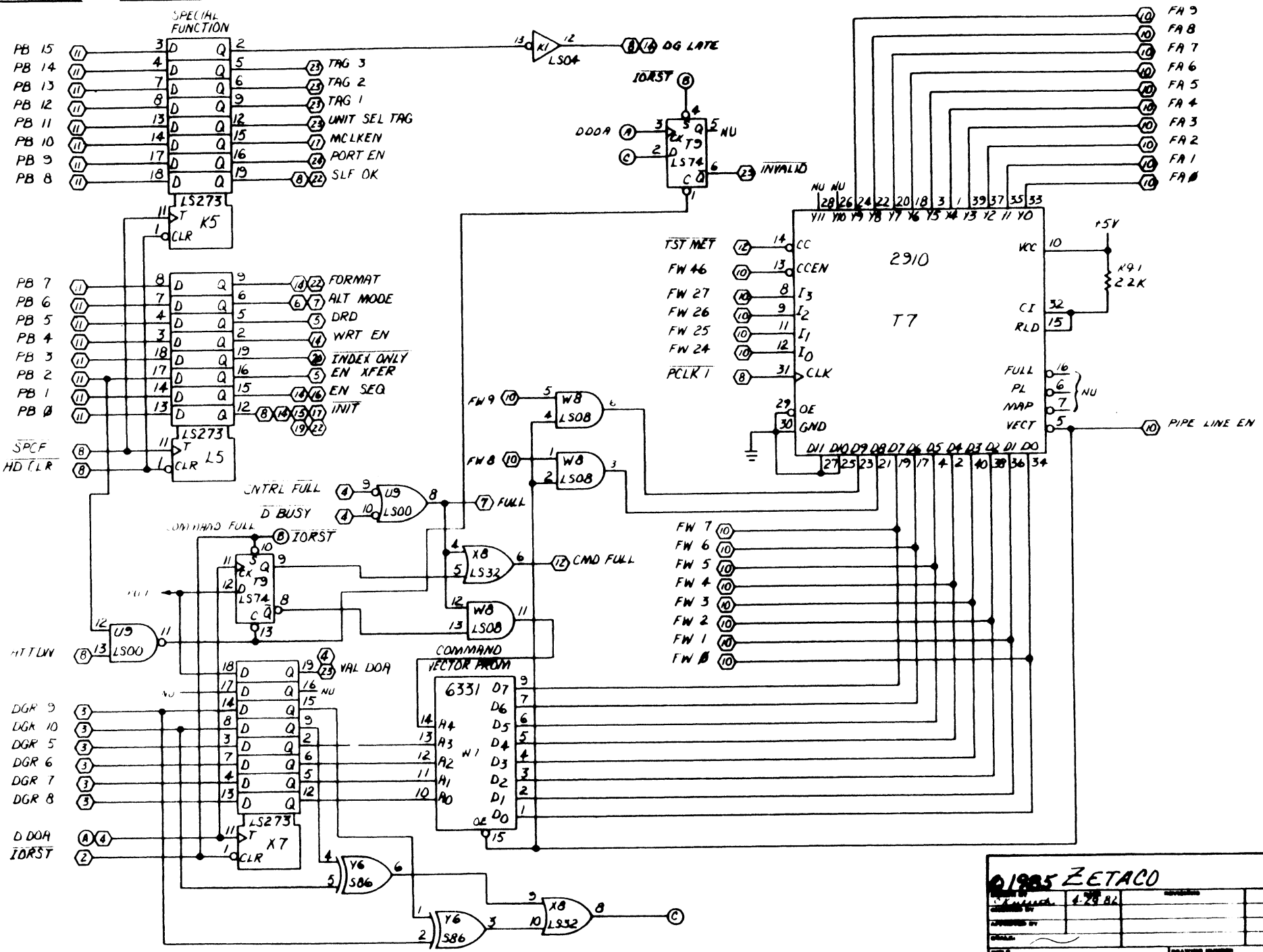
**1985 ZETAC**  
 REGISTER FILE  
 700-383-00C



**01985 ZETACO**

DATE	REV	DESCRIPTION	BY
12/29/86	2		
DESIGNED BY			
DRAWN BY			
CHECKED BY			
DATE			
FILE	DIA DRIVER		700-383-00C

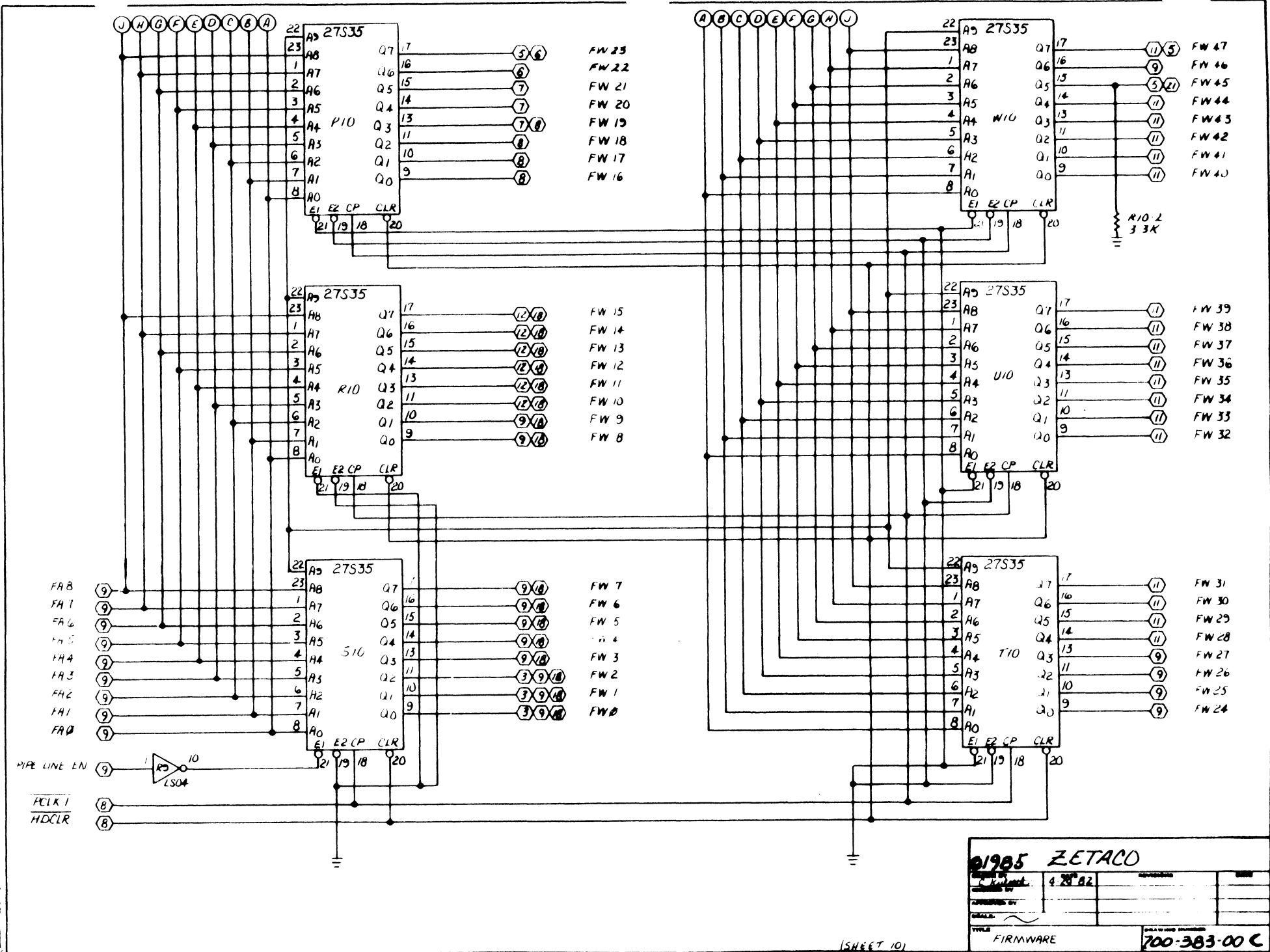




01985 ZETACO

DESIGNED BY	4-28-81	REVISION	
DRAWN BY			
CHECKED BY			
DATE			
FILE	SEQUENCER		
	700-303-00C		

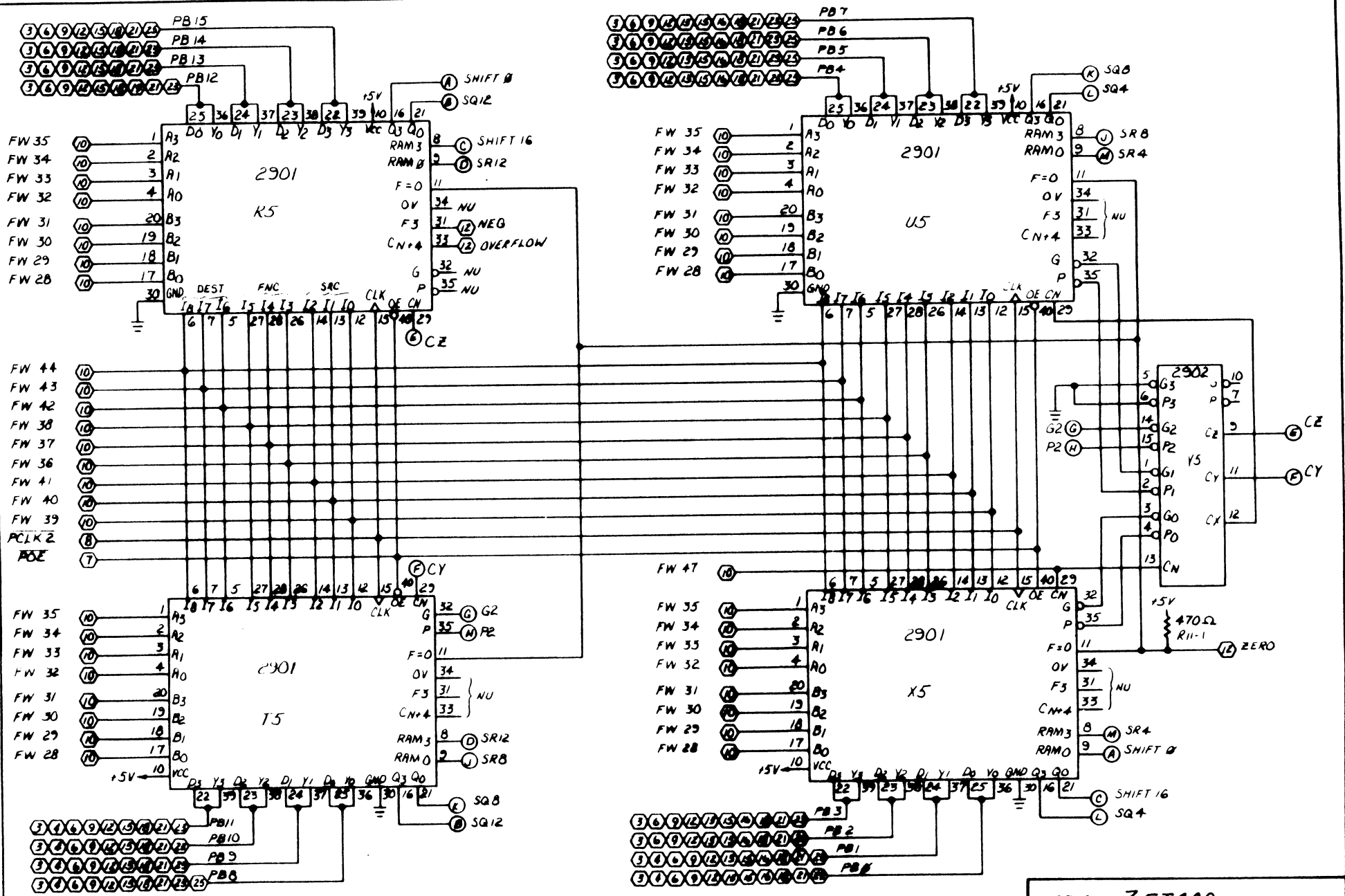
700383-000B



01985 ZETACO	
DATE: 4/28/82	DESIGNED BY:
APPROVED BY:	TESTED BY:
TITLE: FIRMWARE	DATE: 7-10-82
700-383-00 C	

(SHEET 10)

700383-0008



700365 ZETACO	
DATE	1-27-82
DESIGNED BY	
CHECKED BY	
DRG. NO.	
TITLE	PROCESSOR
REVISION NUMBER	700-365-00C

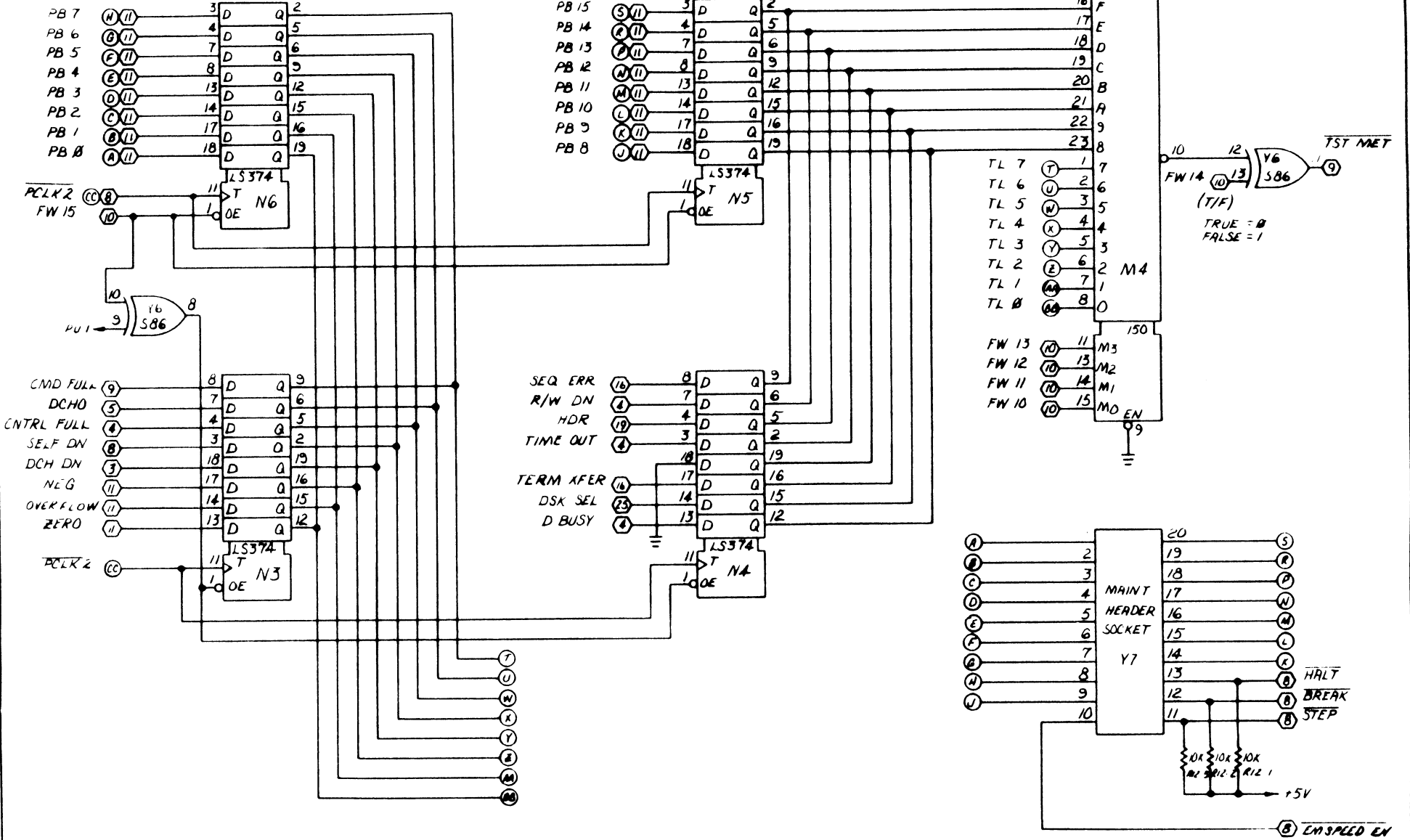
(SHEET 11)

700365-000 B



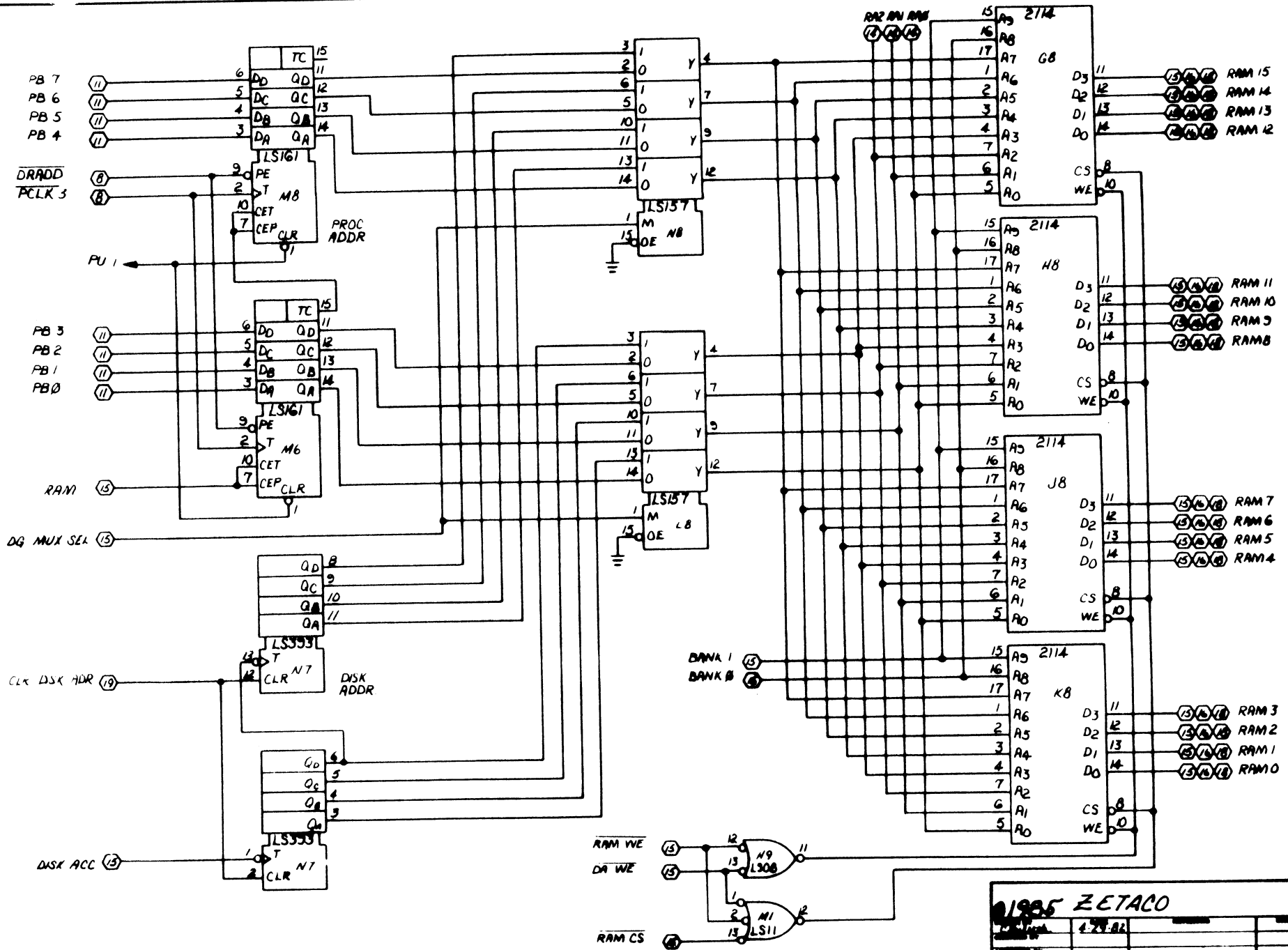
LOWER TEST

UPPER TEST



01285 ZETACO

DATE	1 28 82	REVISED	
DESIGNED BY		TESTED BY	
DRN		DATE	
TEST		TEST CONDITION	700-383-00 C

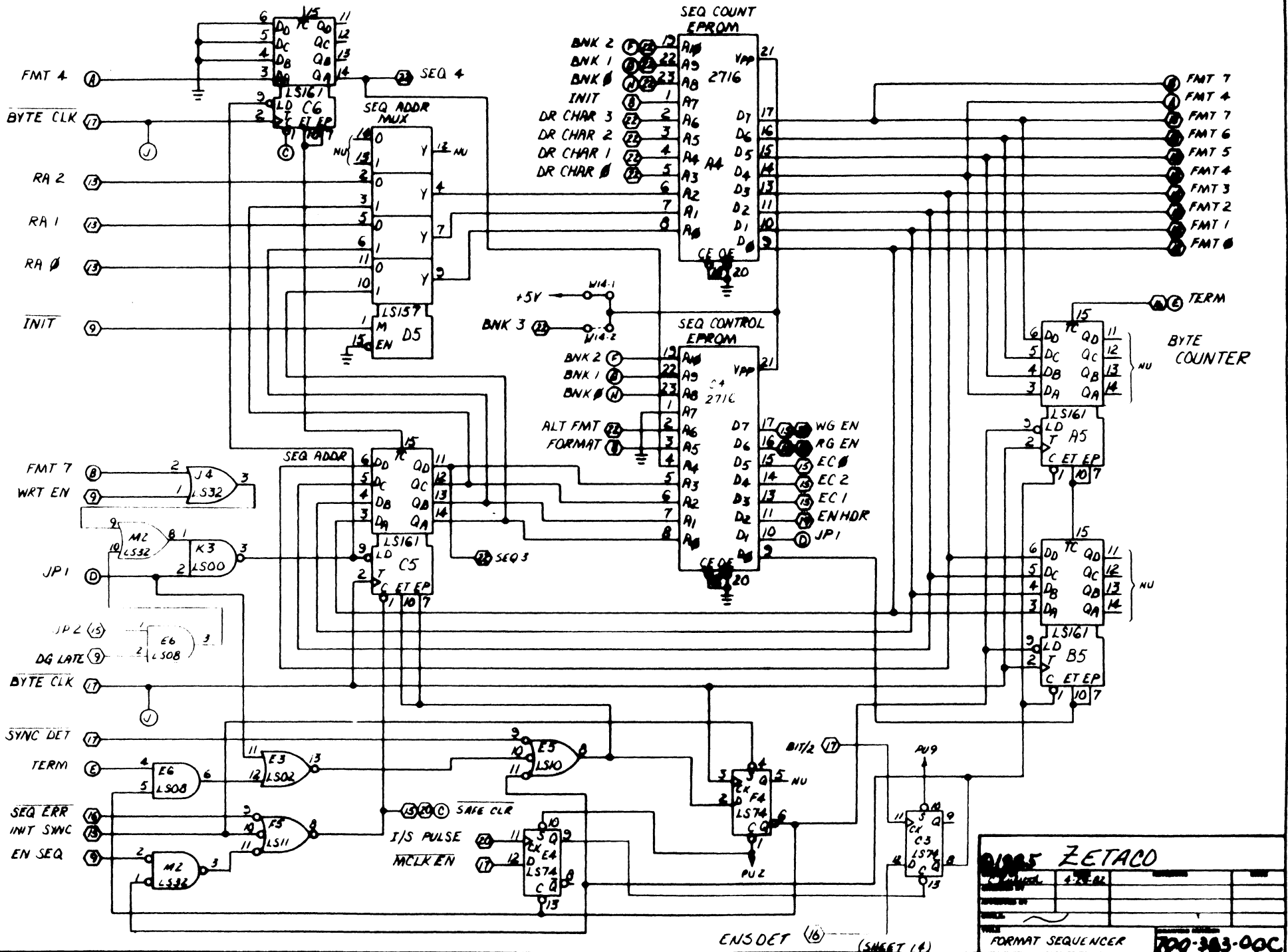


(SHEET 3)

1985 ZETACO

DATE	4-29-82
DESIGNED BY	
CHECKED BY	
APPROVED BY	
MEMORY	700-985-00 C

700383-000B



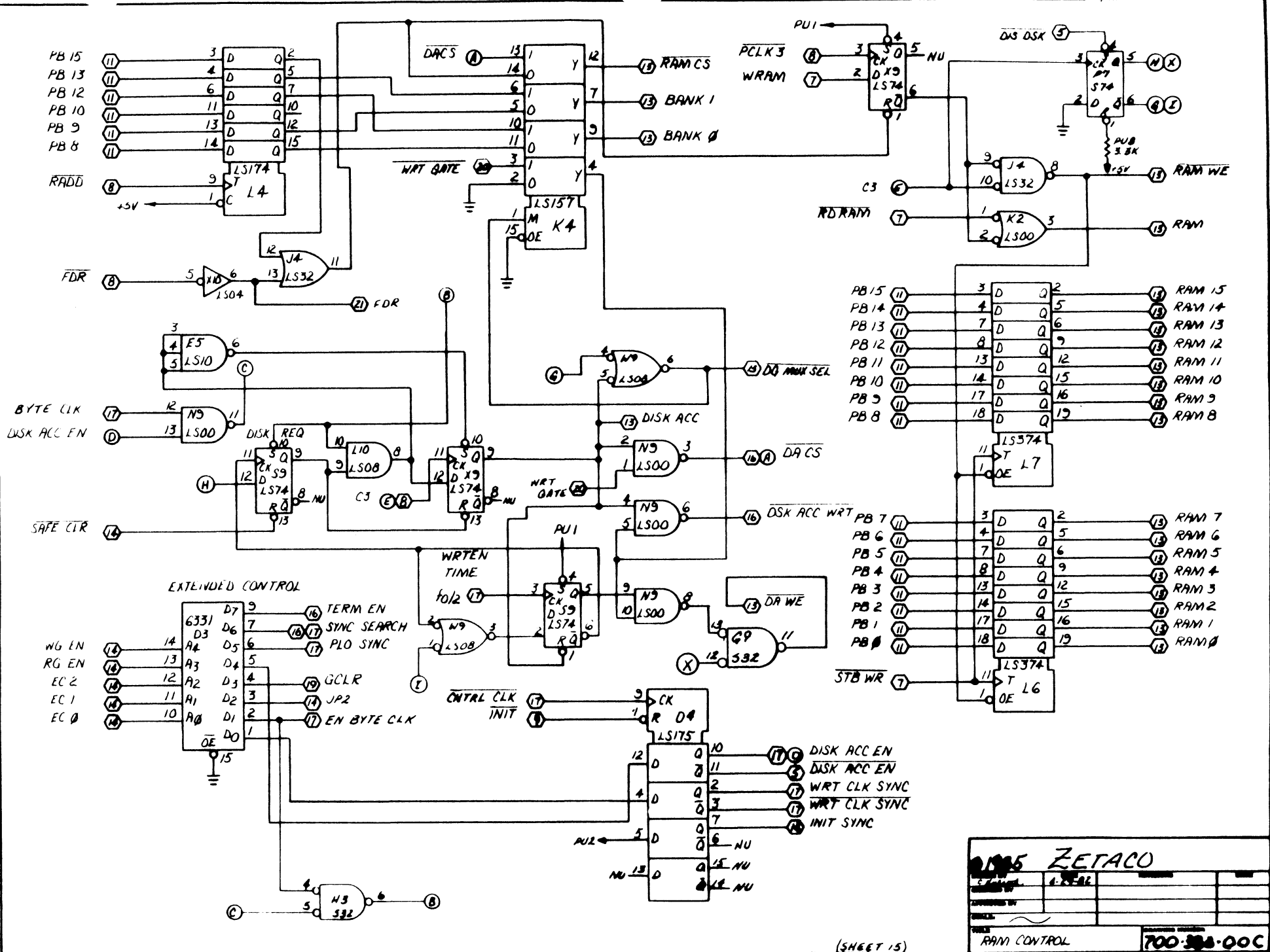
700383-000B

**01005 ZETACO**

REVISED	4-78-82		
DESIGNED BY			
DATE			
CHECKED BY			
DATE			
APPROVED BY			
DATE			

FORMAT SEQUENCER **700-383-000**

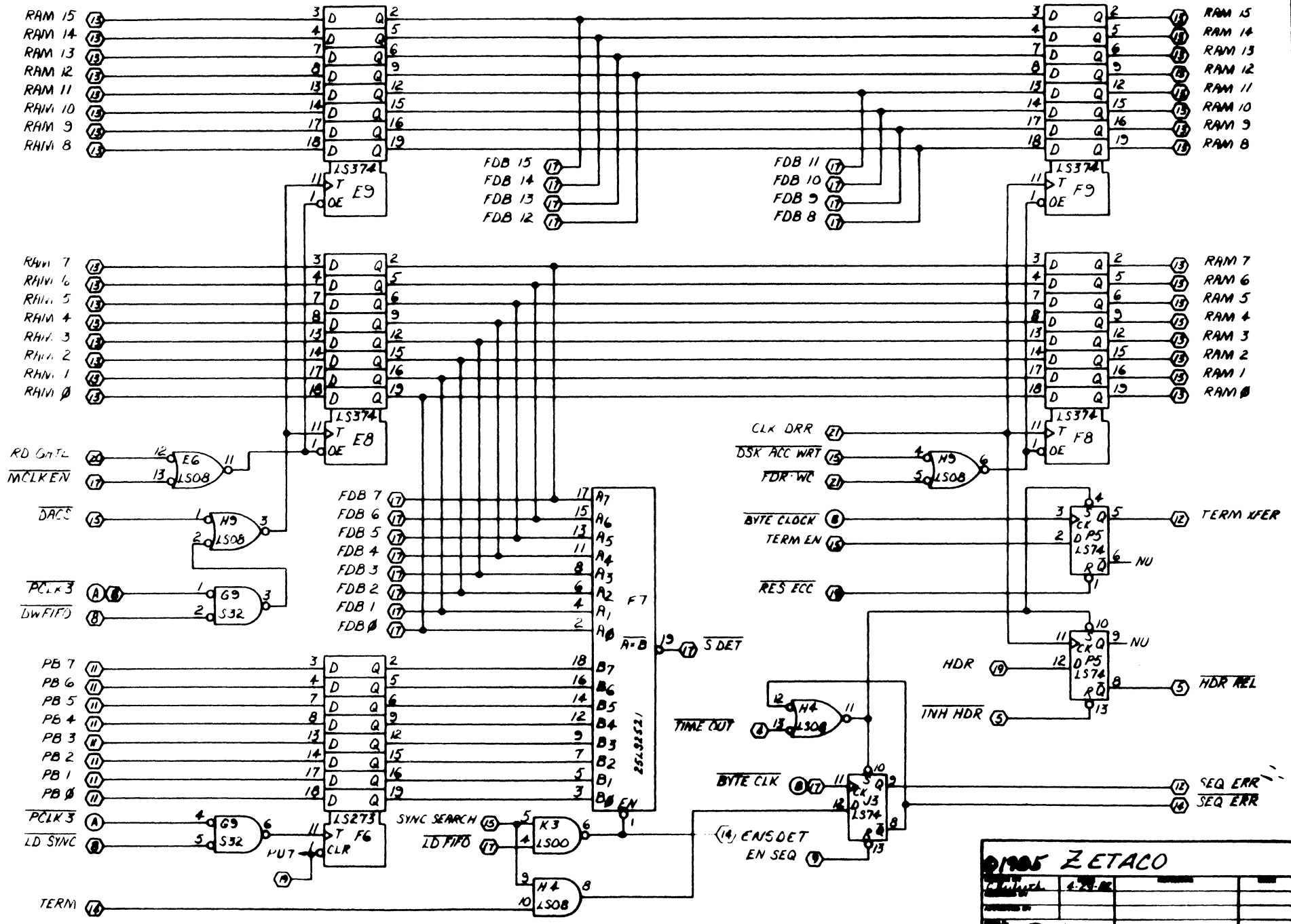
ENSDET (16) (SHEET 18)



4037 TR

<b>0185 ZETACO</b>			
DATE	1-2-82		
DESIGNED BY			
TESTED			
ISSUED			
RAM CONTROL		700-383-000	

DISK WRITE REG



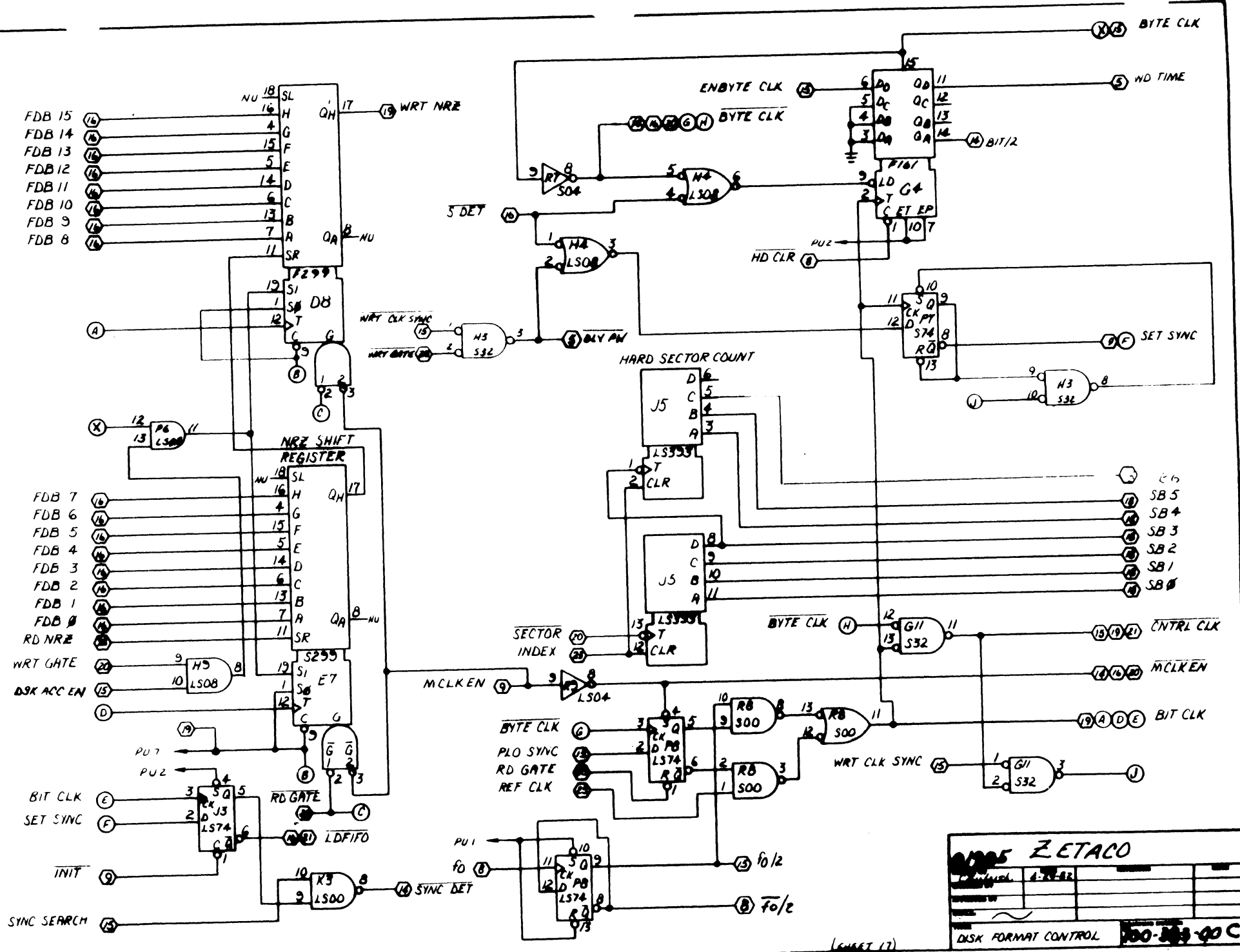
**01905 ZETACO**

DATE	4-28-81
DESIGNED BY	
CHECKED BY	
APPROVED BY	

WITH SYNC DET AND COMMAND BUS REG 700-303-00 C

(SHEET 14)

700383-0008

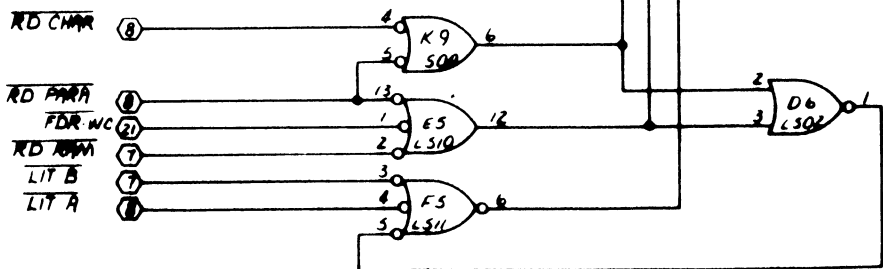
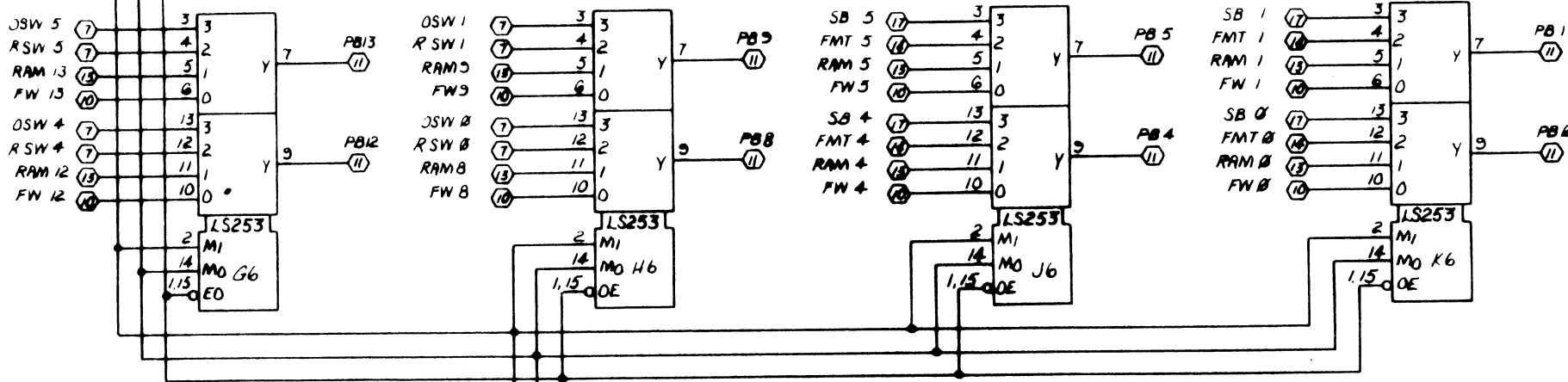
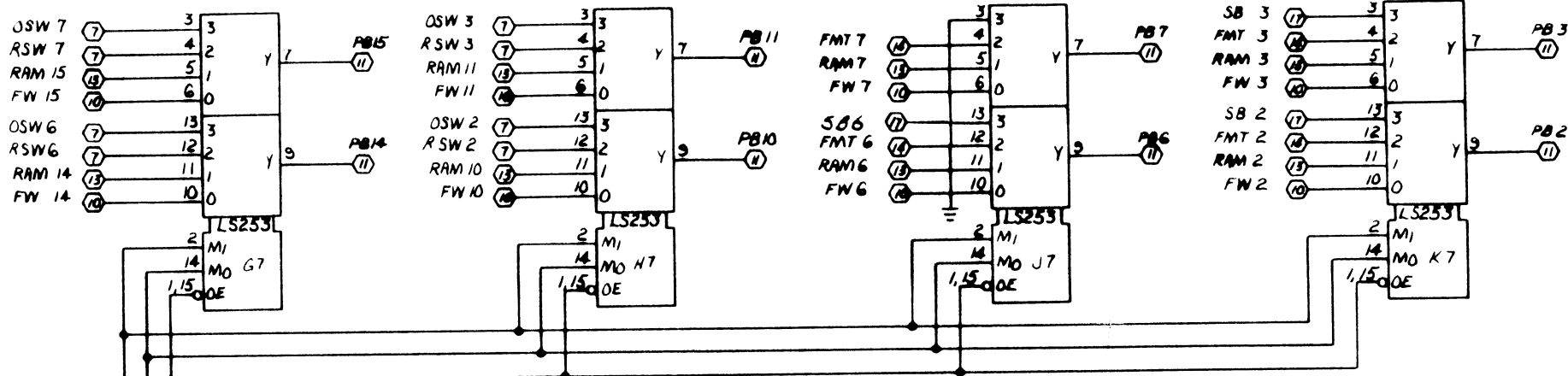


**ZETACO**

Model	4-78-82		
Version			
DISK FORMAT CONTROL			
Part No.	700-383-000C		

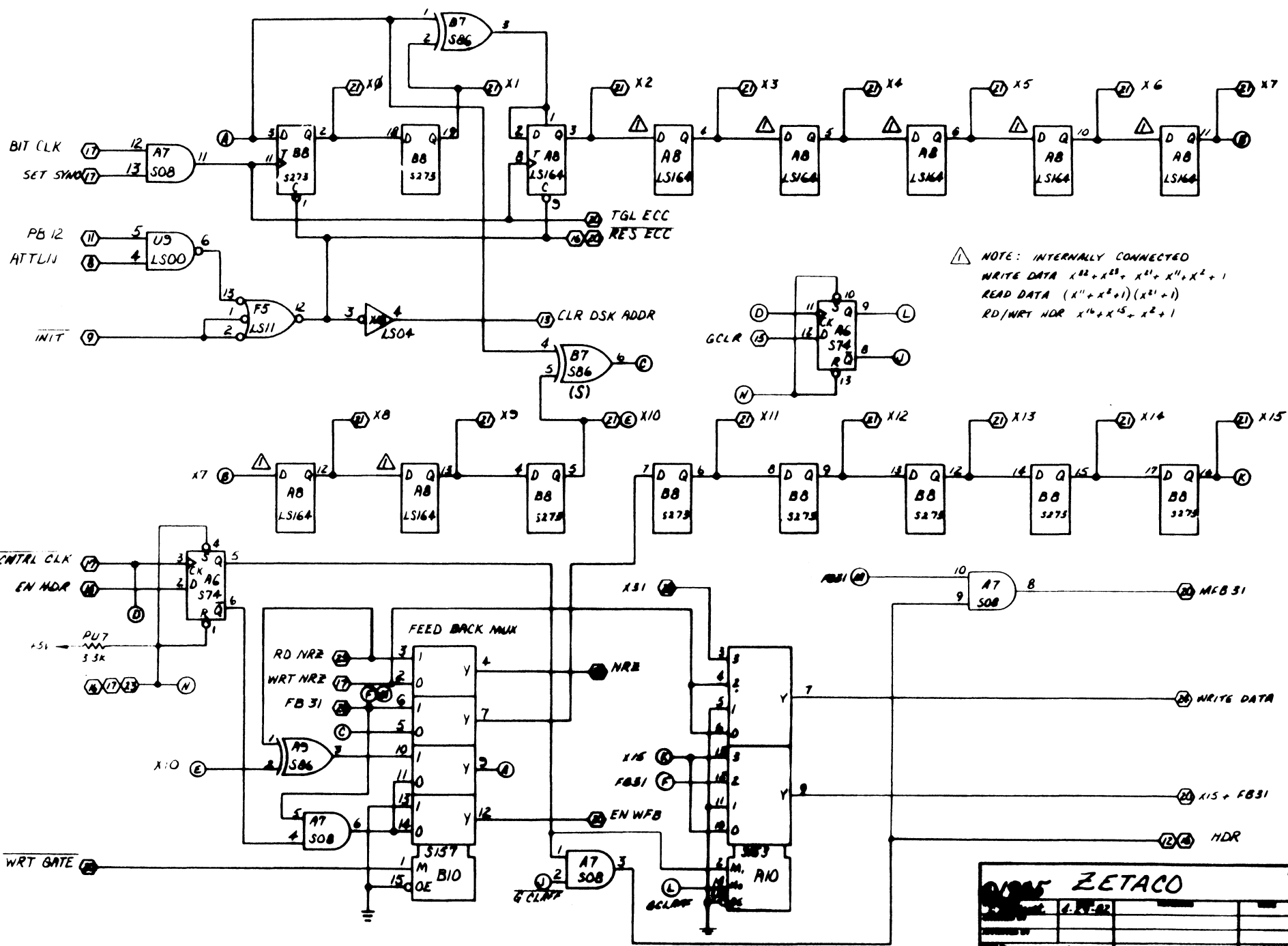
700383-000B

(Sheet 17)



**21905 ZETACO**  
 DATE: 6-29-62  
 DRAWN BY:  
 CHECKED BY:  
 APPROVED BY:  
**PB READ MUX**  
**700-383-00 C**

(SHEET 18)



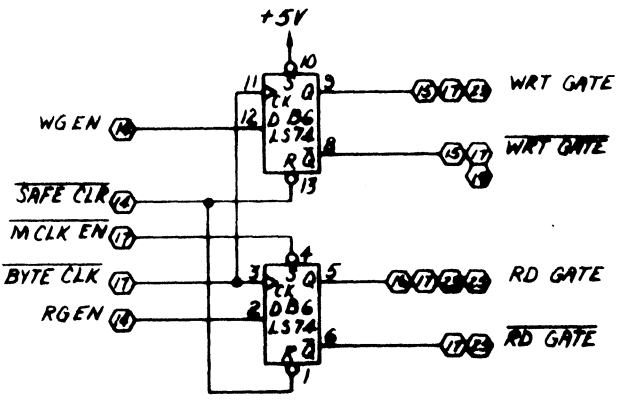
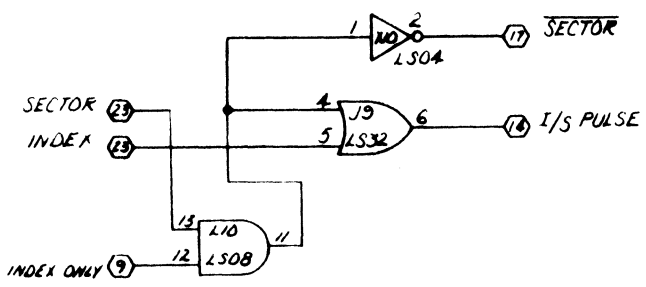
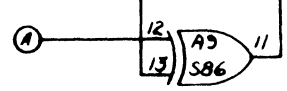
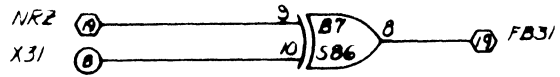
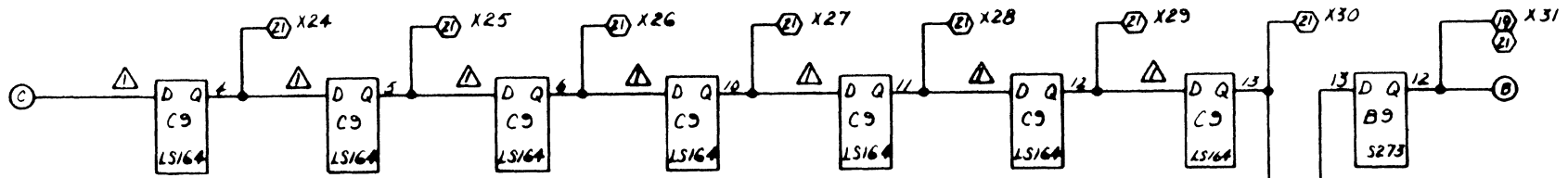
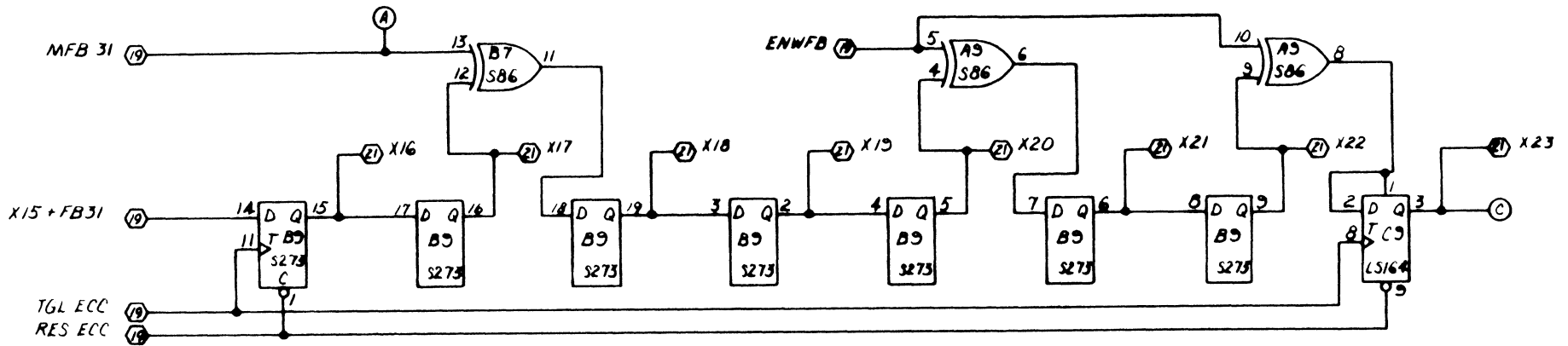
$\Delta$  NOTE: INTERNALLY CONNECTED  
WRITE DATA  $x^{22} + x^{23} + x^{21} + x^{11} + x^2 + 1$   
READ DATA  $(x^{11} + x^2 + 1)(x^{21} + 1)$   
RD/WRT HDR  $x^{14} + x^{15} + x^2 + 1$

700383-000 B

**ZETACO**

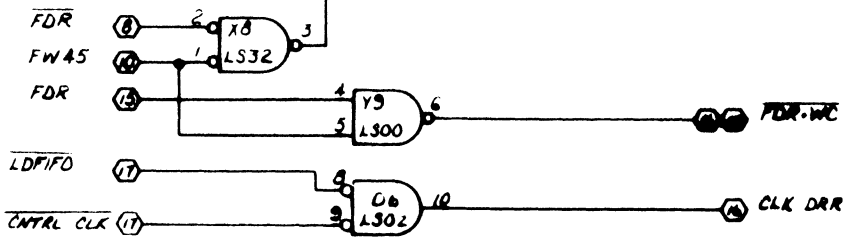
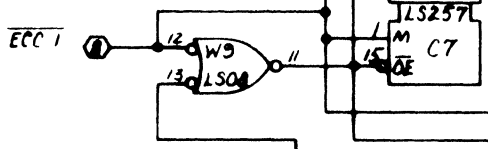
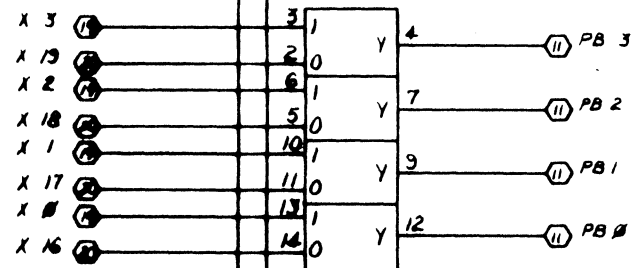
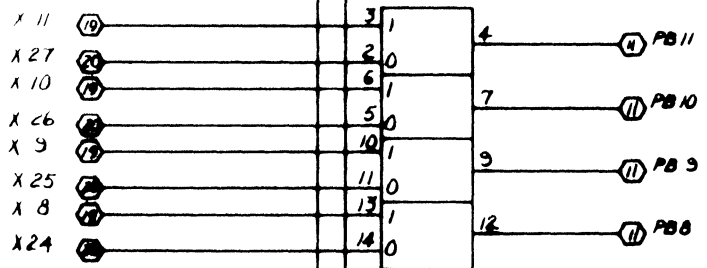
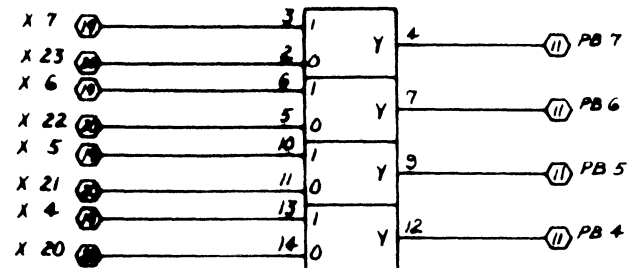
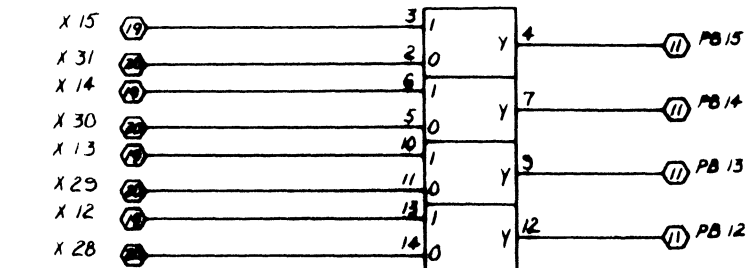
<b>DATE</b> 6-12-82	<b>REV</b> 1	
<b>DESIGNED BY</b>	<b>CHECKED BY</b>	<b>DATE</b>
<b>DRAWN BY</b>	<b>APPROVED BY</b>	<b>DATE</b>
<b>ECC LOWER</b>		
		<b>700-383-000 C</b>





△ NOTE: INTERNALLY CONNECTED

01925 ZETACO	
DATE	1-21-82
DESIGNED BY	
CHECKED BY	
APPROVED BY	
ECC UPPER	
700-303-00 C	



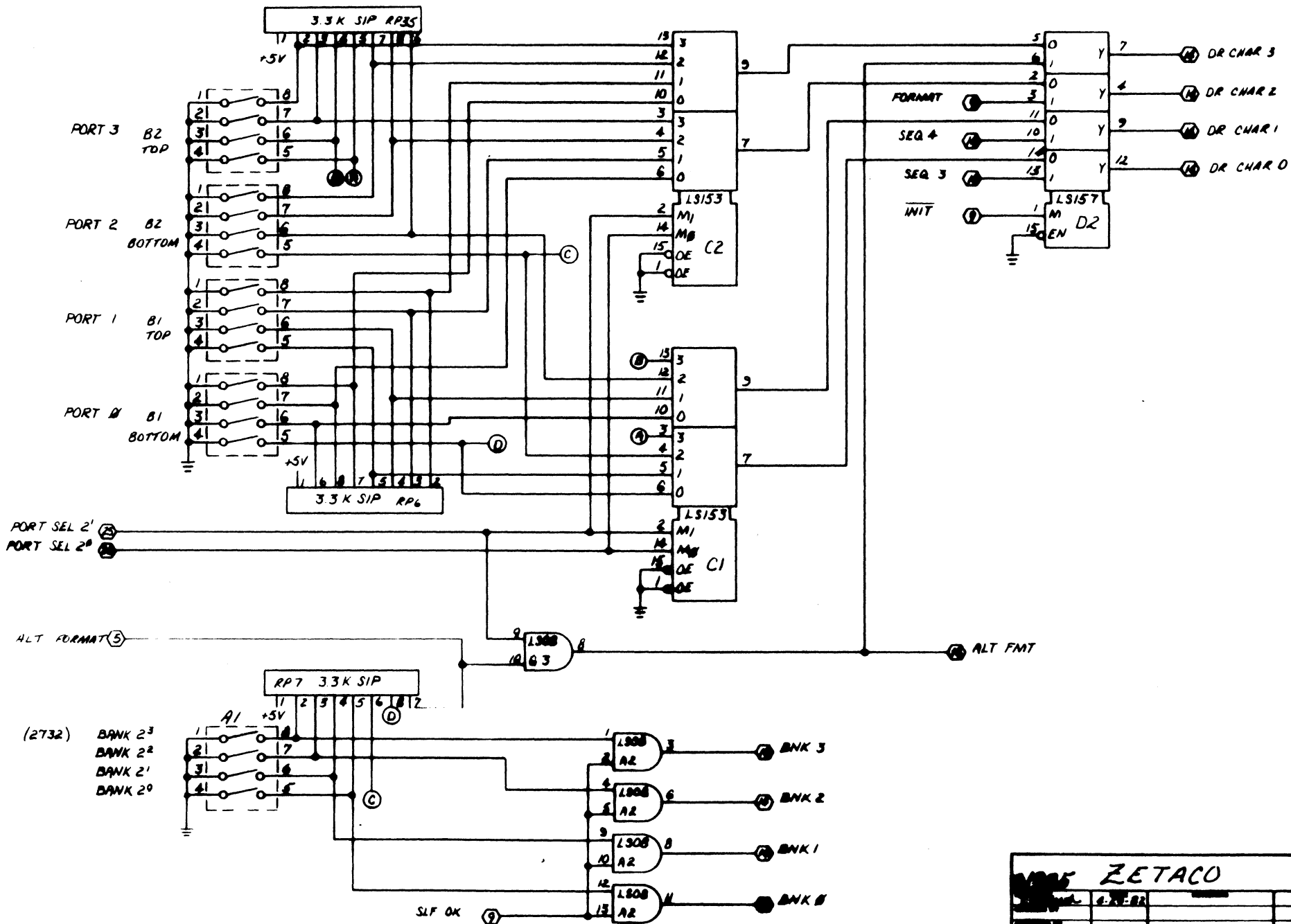
1985 ZETACO

DATE	4-28-82		
DESIGNED BY			
CHECKED BY			
APPROVED BY			

ECC OUT PUT SELECT 700-383-00 C

700383-000 B

(PAGE 21)



ZETACO			
DATE	6-27-82		
DESIGNED BY			
CHECKED BY			
FORMAT BANK SELECT 700-383-000 C			

INDEX  
INDEX  
SECTOR  
SECTOR  
FAULT  
FAULT  
SEEK ERR  
SEEK ERR

ON CYL  
ON CYL  
UNIT RDY  
UNIT RDY  
WR PROT  
WR PROT  
BUSY  
BUSY

PB 3  
PB 2  
PB 1  
PB 0

PCK 3  
SYB CMD  
HDC LR

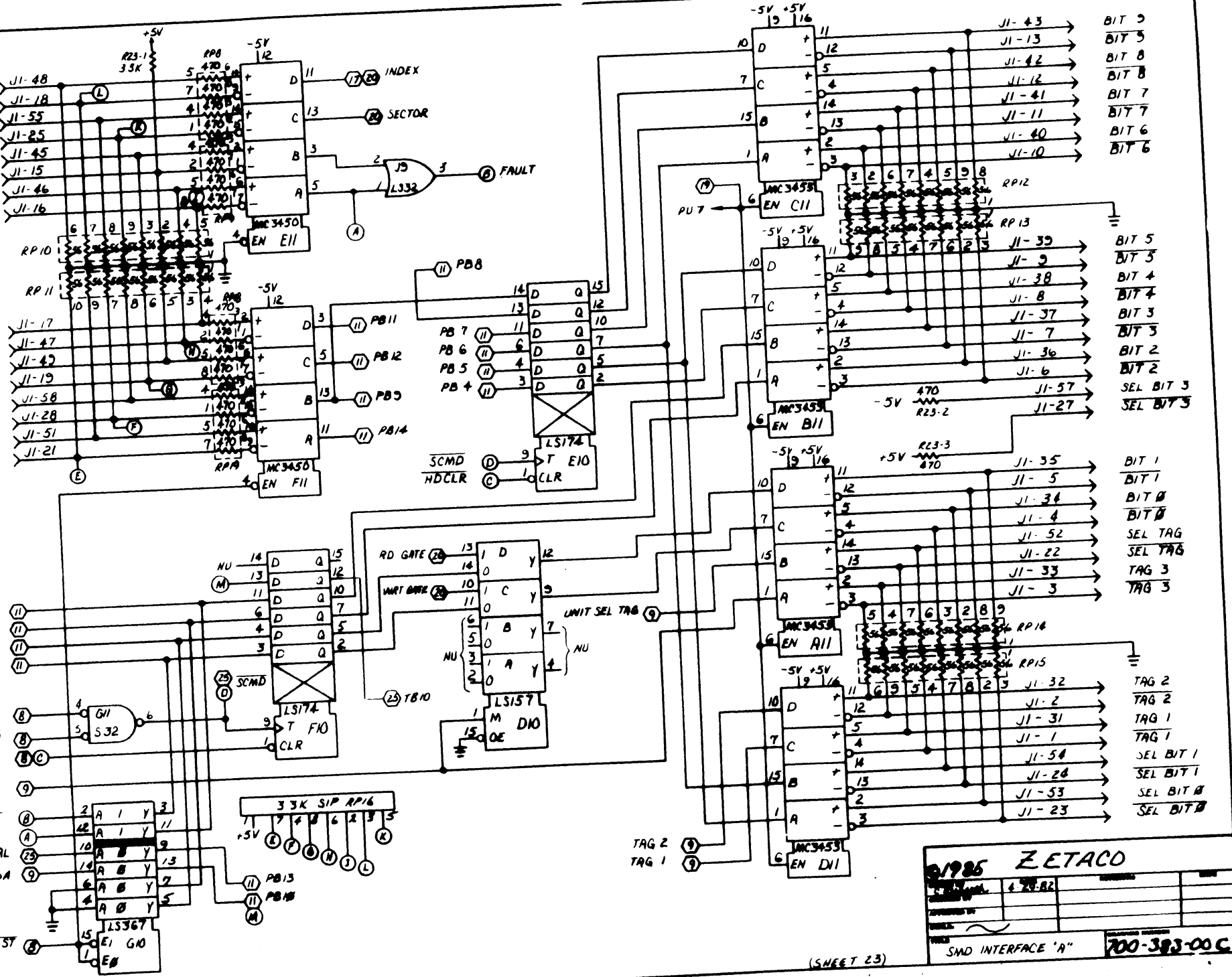
TAG 3

FAULT

DOC VAL

VAL DOA

RD SWD ST



BIT 9  
BIT 8  
BIT 8  
BIT 8  
BIT 7  
BIT 7  
BIT 6  
BIT 6

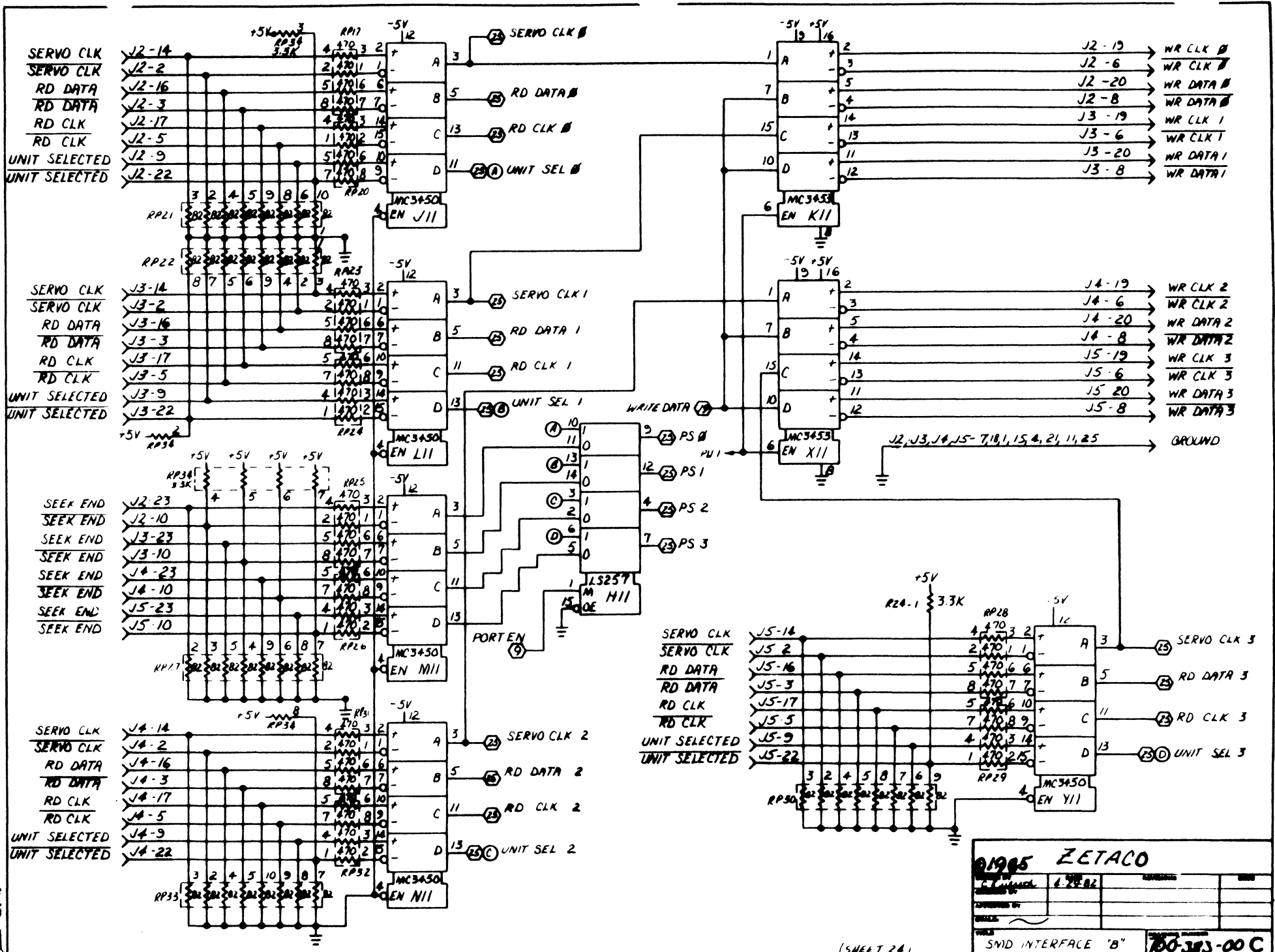
BIT 5  
BIT 5  
BIT 4  
BIT 4  
BIT 3  
BIT 3  
BIT 2  
BIT 2  
SEL BIT 3  
SEL BIT 5

BIT 1  
BIT 1  
BIT 0  
BIT 0  
SEL TAG  
SEL TAG  
TAG 3  
TAG 3

TAG 2  
TAG 2  
TAG 1  
TAG 1  
SEL BIT 1  
SEL BIT 1  
SEL BIT 0  
SEL BIT 0

01/985 ZETACO

DATE	4-28-82	DESIGNER	
APPROVED BY			
SMD INTERFACE 'A'			
			700-383-00C

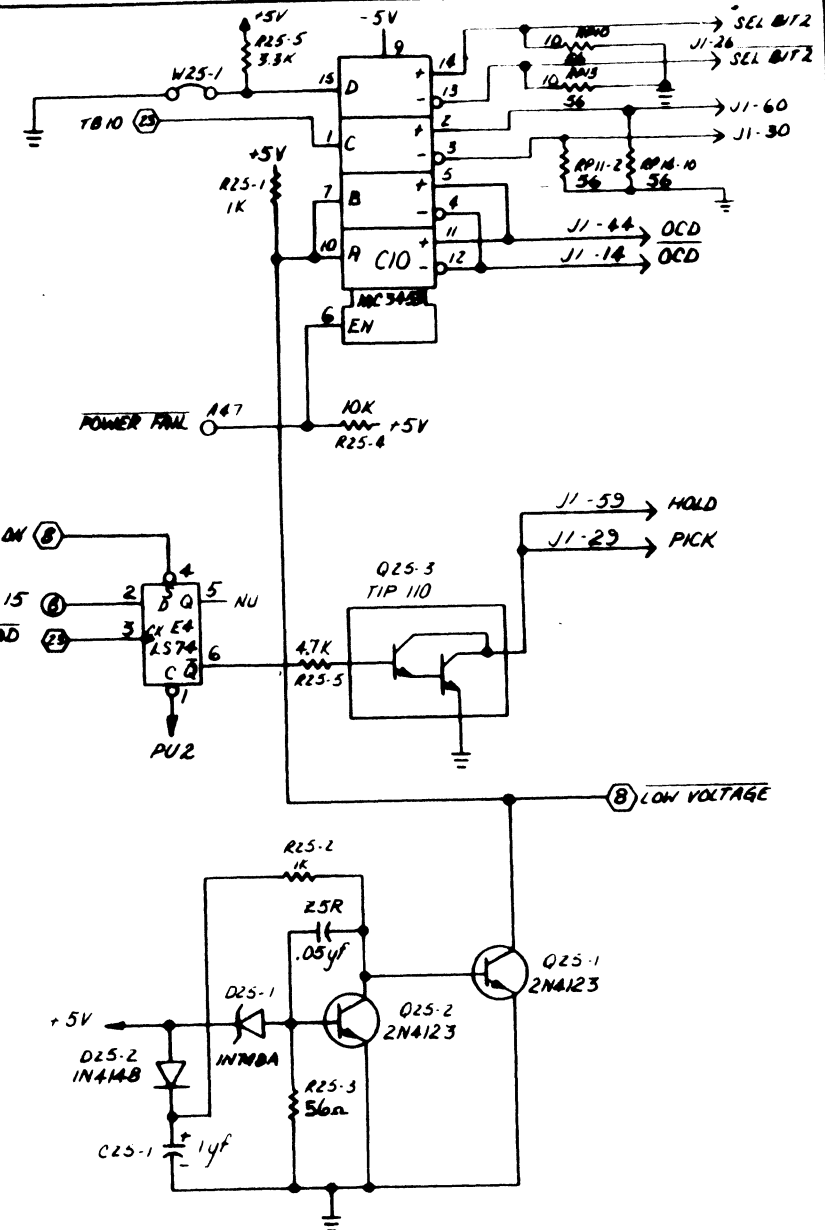
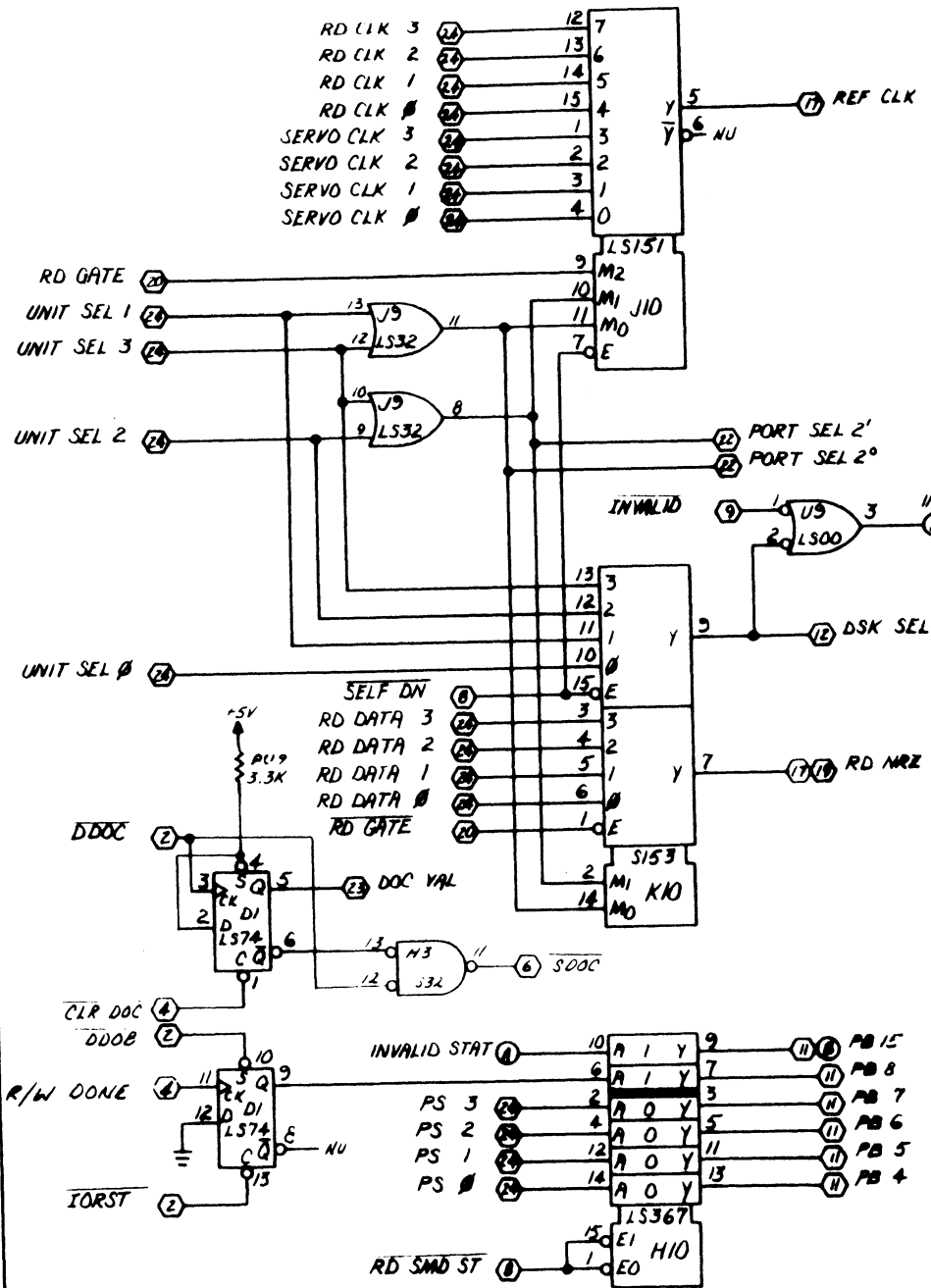


01905 ZETACO	
DATE	4-28-82
DESIGNED BY	
CHECKED BY	
DATE	
SMD INTERFACE "B"	
700383-00C	

(SHEET 24)

700383-000B

403179



01985 ZETACO

DATE	4-28-82		
DESIGNED BY			
CHECKED BY			
FILE			
SMD INTERFACE CONTROL	700-383-00C		